PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Supplement to
Book IC11 1988

Linear Products

SUPPLEMENT

LINEAR PRODUCTS

SELECTION GUIDE

Numerical index

NUMERICAL INDEX

GENERAL

Type designation

Rating systems

Handling MOS devices

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

STEPPING MOTOR DRIVE CIRCUIT

GENERAL DESCRIPTION

The SAA1027 is a bipolar integrated circuit intended for driving a four-phase two-stator motor. The circuit consists of a bidirectional four-state counter and a code converter to drive the four outputs in the sequence required for driving a stepping motor.

Features

- High noise immunity inputs
- Clockwise and counter-clockwise operation
- Reset facility
- High output current
- Outputs protected against damage by overshoot.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	9,5 to 18	V
Supply current, unloaded	I_{CC}	typ. 4,5	mA
Input voltage, all inputs			
HIGH	V_{IH}	min. 7,5	V
LOW	V_{IL}	max. 4,5	V
Input current, all inputs, LOW	I_{IL}	typ. 30	μA
Output current LOW	I_{OL}	max. 500	mA
Operating ambient temperature range	T_{amb}	−20 to +70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38A).

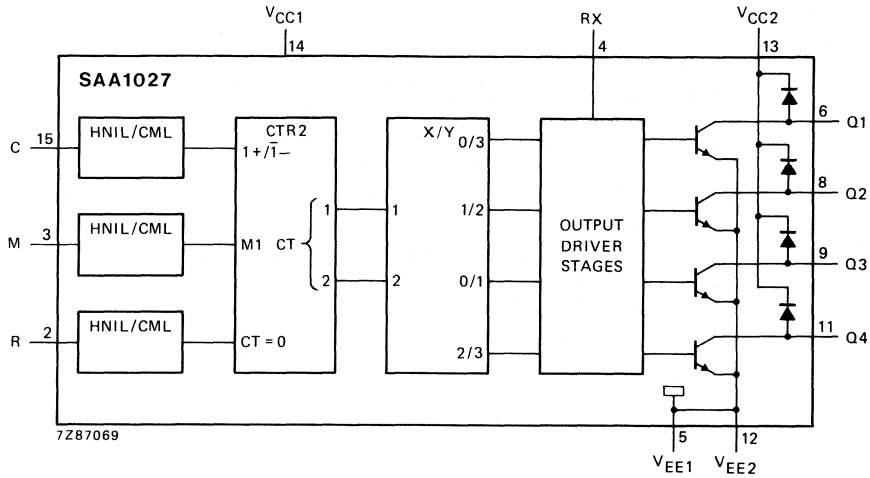


Fig. 1 Block diagram. The blocks marked HNIL/CML are high noise immunity input stages, the block marked CTR2 is a bidirectional synchronous 2-bit (4-state) counter and the block marked X/Y is a code converter. C is the count input, M the mode input to select forward or reverse counting and R is the reset input which resets the counter to content zero.

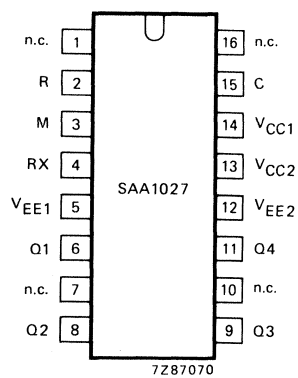


Fig. 2 Pinning diagram.

PINNING

1	n.c.	not connected
2	R	reset input
3	M	mode input
4	RX	external resistor
5	V_{EE1}	ground
6	Q1	output 1
7	n.c.	not connected
8	Q2	output 2
9	Q3	output 3
10	n.c.	not connected
11	Q4	output 4
12	V_{EE2}	ground
13	V_{CC2}	positive supply
14	V_{CC1}	positive supply
15	C	count input
16	n.c.	not connected

FUNCTIONAL DESCRIPTION

Count input C (pin 15)

The outputs change state after each L to H signal transition at the count input.

Mode input M (pin 3)

With the mode input the sequence of output signals, and hence the direction of rotation of the stepping motor, can be chosen, as shown in the following table.

counting sequence	M = L				M = H			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
0	L	H	L	H	L	H	L	H
1	H	L	L	H	L	H	H	L
2	H	L	H	L	H	L	H	L
3	L	H	H	L	H	L	L	H
0	L	H	L	H	L	H	L	H

Reset input R (pin 2)

A LOW level at the R input resets the counter to content zero. The outputs take on the levels shown in the upper and lower line of the table above.

If this facility is not used the R input should be connected to the supply.

External resistor pin RX (pin 4)

The external resistor R4 connected to RX sets the base current of the output transistors. Its value has to be chosen in accordance with the required output current (see Fig. 5).

Outputs Q1 to Q4 (pins 6, 8, 9 and 11)

The circuit has open-collector outputs. To prevent damage by an overshooting output voltage the outputs are protected by diodes connected to V_{CC2}, pin 13. High output currents mainly determine the total power dissipation, see Fig. 3.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC1}; V_{CC2}	max.	18	V
Input voltage, all inputs	V_I	max.	18	V
Current into pin 4	I_{RX}	max.	120	mA
Output current	I_{OL}	max.	500	mA
Power dissipation	P_{tot}	see Fig. 4		
Storage temperature range	T_{stg}	−40 to +125		°C
Operating ambient temperature range	T_{amb}	−20 to +70		°C

CHARACTERISTICS

V_{CC} = 9,5 to 18 V; V_{EE} = 0 V; T_{amb} = −20 to 70 °C unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC1} and V_{CC2} (pins 14 and 13)					
Supply current at V_{CC1} = 12 V; unloaded; all inputs HIGH; pin 4 open	I_{CC}	2	4,5	6,5	mA
Inputs C, M and R (pins 15, 3 and 2)					
Input voltage					
HIGH	V_{IH}	7,5	–	–	V
LOW	V_{IL}	–	–	4,5	V
Input current					
HIGH	I_{IH}	–	1	–	μA
LOW	$-I_{IL}$	–	30	–	μA
External resistor pin RX (pin 4)					
Voltage at RX at V_{CC} = 12 V ± 15%; R4 = 130 Ω ± 5%	V_{RX}	3	–	4,5	V
Outputs Q1 to Q4					
Output voltage LOW					
at I_{OL} = 350 mA	V_{OL}	–	500	1000	mV
at I_{OL} = 500 mA	V_{OL}	–	700	–	mV
Output current					
LOW	I_{OL}	–	–	500*	mA
HIGH at V_Q = 18 V	$-I_{OH}$	–	–	50	μA

* See Figs 3 and 4.

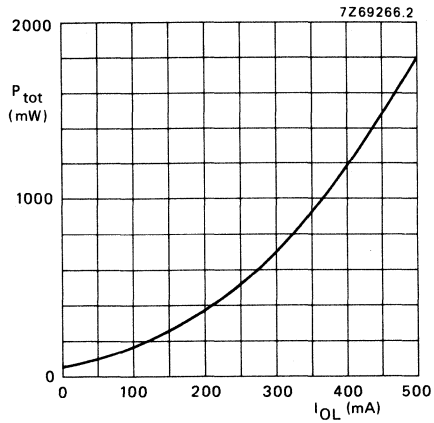


Fig. 3 Total power dissipation P_{tot} as a function of output current I_{OL}.

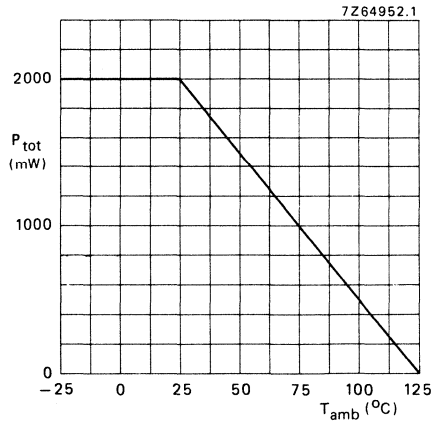


Fig. 4 Power derating curve.

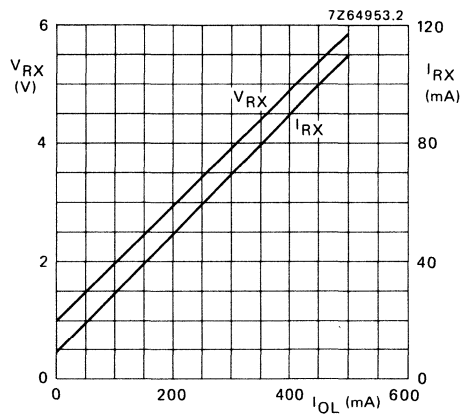


Fig. 5 Current I_{RX} into RX and voltage V_{RX} on RX as a function of required output current I_{OL}.

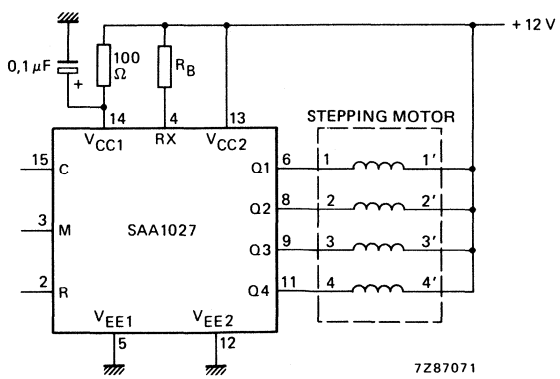


Fig. 6 Typical application of the SAA1027 as a stepping motor driver.

UNIVERSAL INDUSTRIAL LOGIC AND INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1029 is a universal bipolar logic and interface IC with high noise immunity and operational stability for industrial control applications. The most fundamental industrial control functions can be accomplished with only one SAA1029 IC. Figure 1 shows the logic configuration.

The IC comprises,
(1) Gate 1: 4-input AND gate with 1 inverted input,
(2) Gate 2: 3-input AND gate with 1 inverted input and adjustable propagation delay,
(3) Gate 3: 2-input AND gate with 1 inverted input.
The SAA1029 can be used as direct interface with LOCMOS (CMOS) ICs for realizing more complex functions. Therefore, the output signal can be limited to the voltage level of the common output clamping pin Z.

The propagation delay of NAND gate 2 is adjustable from microseconds to seconds by using an external capacitor at pin C. This makes it possible to adapt the control frequency limits to the system, so the optimum dynamic noise immunity can be achieved.

All the static and dynamic circuit values (including the output voltage) are independent of the supply voltage over a wide operating range. This allows the use of a simple unstabilized power supply.

The output is held to the LOW state automatically during switching on the power supply, so a special reset pulse can be omitted.

Features

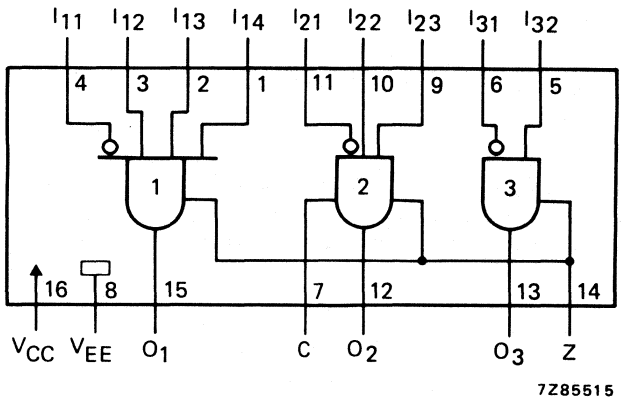
- Simple realization of the basic industrial control functions (logic functions, timing functions, memory functions).
- High dynamic and static noise immunity.
- High operation stability.
- Short-circuit protection of inputs and outputs to both V_{EE} and V_{CC}.
- Wide supply voltage range, so a simple power supply can be used.
- Wire interruption results in a safe input LOW state.
- LOCMOS (CMOS) compatible.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}	14 to 31,2	V
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Input voltage HIGH	V_{IH}	6,5 to 44	V
Output voltage HIGH (without clamping)	V_{OH}	13 to 30	V
Output voltage HIGH (with clamping at pin Z)	V_{OH}	2,0 to (V_{CC} −0,7)	V
Input current	I_I	max. 10	mA
Quiescent supply current	I_{CC}	typ. 7,8	mA

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



Logic equations:

$O_1 = \overline{I_{11}} \cdot I_{12} \cdot I_{13} \cdot I_{14}$

$O_2 = \overline{I_{21}} \cdot I_{22} \cdot I_{23}$

$O_3 = \overline{I_{31}} \cdot I_{32}$

Fig. 1 Logic diagram.

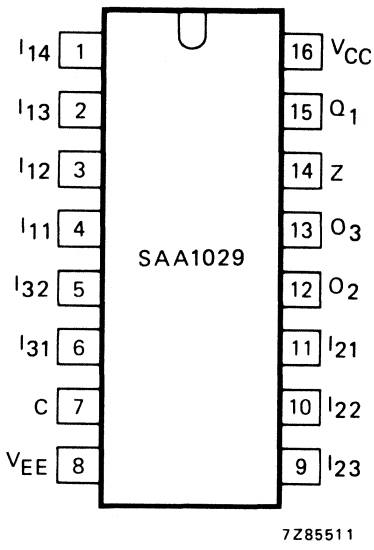


Fig. 2 Pinning diagram.

PINNING

4	I_{11}	inputs of gate 1
3	I_{12}	
2	I_{13}	
1	I_{14}	
15	O_1	output of gate 1
11	I_{21}	inputs of gate 2
10	I_{22}	
9	I_{23}	
12	O_2	output of gate 2
6	I_{31}	inputs of gate 3
5	I_{32}	
13	O_3	output of gate 3
7	C	external delay capacitor
14	Z	common output clamping
16	V_{CC}	positive supply voltage
8	V_{EE}	ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}		0 to + 35	V
Input voltage (independent of V_{CC})	V_I		−0,15 to + 44	V
Output clamping voltage (pin 14)	V_Z		0 to + 35	V
Voltage at any output (pins 12, 13 and 15)				
pin 14 (Z) open	V_O		−0,15 to V_{CC}	V
pin 14 (Z) at V_Z	V_O	max.	V_Z or V_{CC} if $V_{CC} < V_Z$	V
Current into any input				
d.c.	$\pm I_I$	max.	10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{IM}$	max.	100	mA
Sum of input currents				
d.c.	ΣI_I		−90 to + 10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	ΣI_{IM}		−900 to + 300	mA
External applied current at any output (pins 12, 13 and 15)				
pin 14 (Z) open				
d.c.	$\pm I_O$	max.	30	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	$\pm I_{OM}$	max.	500	mA
External applied current at any output (pins 12, 13 and 15)				
pin 14 (Z) at V_Z				
d.c.	I_O		−30 to + 10	mA
t_p = 0,5 μs; δ = 0,1% (peak value)	I_O		−500 to + 100	mA
Voltage at pin 7 (C)	V_C		−0,15 to + 6	V
External capacitor at pin 7 (C)	any value			
Short-circuit of outputs (pins 12, 13 and 15)				
pin 14 (Z) open	allowed to V_{CC} and V_{EE} (0 V)			
at $V_Z < V_{CC}$	allowed only to V_{EE} (0 V)			
Total power dissipation (see also Fig. 3)				
at T_{amb} = 50 °C; continuous	P_{tot}	max.	1100	mW
at T_{amb} = 65 °C; max. 1000 hours	P_{tot}	max.	1100	mW
Storage temperature range	T_{stg}		−40 to + 150	°C

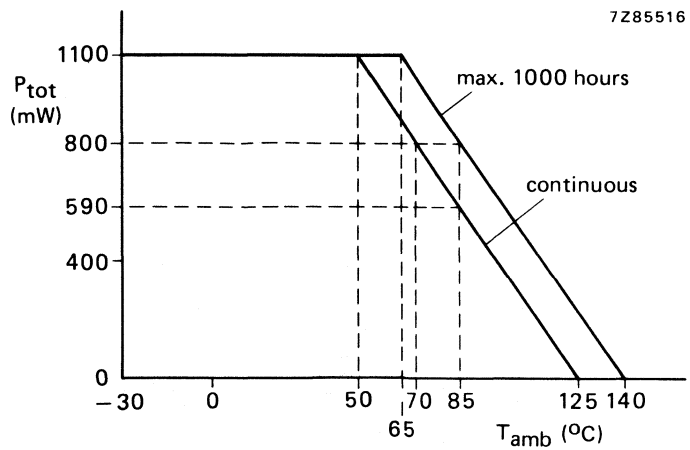


Fig. 3 Power derating curves; $R_{th\ j\text{-}a}$ = 70 K/W.

CHARACTERISTICS

At T_{amb} = −30 to + 85 °C; $T_j \leqslant$ 125 °C; V_{CC} = 14 to 31,2 V; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{CC}	14	24	31,2	V
Quiescent supply current		I_{CC}	–	7,8	–	mA
	V_{CC} = 31 V; T_{amb} = 25 °C	I_{CC}	–	–	12,2	mA
Quiescent current ratio	I_{CC1} = I_{CC} at T_j = 125 °C I_{CC2} = I_{CC} at T_j = 25 °C	$\frac{I_{CC1}}{I_{CC2}}$	–	0,67	–	
Input voltage LOW		V_{IL}	–	–	5	V
Input voltage HIGH		V_{IH}	6,5	–	–	V
		V_{IH}	6,55	–	–	V
Input current LOW		$-I_{IL}$	–	–	100	μA
		$-I_{IL}$	–	–	95	μA
Input current HIGH		I_{IH}	300	–	–	μA
Rate of change of input signal		dV/dt	3	–	–	V/ms
Input current*	V_I = 1 V	$-I_I$	–	–	120	μA
	V_I = 35 V	I_I	–	–	280	μA
Output clamping voltage*	$V_Z = V_{CC} - 1$ V	V_Z	–	–	30	V
Output voltage without clamping (pin 14 open)* non-inverting input: V_I = 5,1 V inverting input: V_I = 6,3 V	V_{CC} = 14 V					
LOW	I_O = 1,32 mA	V_{OL}	–	–	1	V
	I_O = 2,91 mA	V_{OL}	–	–	1,5	V
HIGH	$-I_O$ = 5 mA	V_{OH}	$V_{CC}-1,4$	–	–	V
Output voltage with clamping (pin 14 at V_Z)*	V_{CC} = 31,2 V $V_Z < V_{CC}-1$ V					
LOW	I_O = 1,32 mA	V_{OL}	–	–	1	V
	I_O = 1,91 mA	V_{OL}	–	–	1,5	V

* At T_{amb} = 25 °C; V_{CC} = 24 V; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
HIGH	I_O = 0 mA	V_{OH}	(V_Z −0,475)	–	(V_Z + 0,225)	V
	$-I_O$ = 1 mA	V_{OH}	(V_Z −0,455)	–	(V_Z + 0,12)	V
	$-I_O$ = 3 mA	V_{OH}	(V_Z −0,41)	–	(V_Z + 0,055)	V
Output short-circuit current*						
LOW-signal	output at V_{CC}	I_{OscL}	2,95	–	9,6	mA
HIGH-signal	output at V_{EE} (0 V)	$-I_{OscH}$	10,1	–	21,9	mA
Capacitor charging current*		I_C	–	30	–	μA
Propagation delays*						
gates 1, 2 and 3						
HIGH to LOW	C = 0 (at gate 2)	t_{PHL}	–	3,5	–	μs
LOW to HIGH		t_{PLH}	–	3,5	–	μs
gate 2						
HIGH to LOW	C = 47 nF ± 1%	t_{PHL}	1,85	–	5,2	ms
LOW to HIGH	$R_{insulation} > 100$ MΩ	t_{PLH}	7,5	–	14	ms

* At T_{amb} = 25 °C; V_{CC} = 24 V; unless otherwise specified.

CHARACTERISTICS (worst case conditions)

At T_j = + 125 to + 140 °C; maximum 1000 hours

parameter	conditions	symbol	min.	typ.	max.	unit
Input voltage LOW		V_{IL}	–	–	5	V
Input voltage HIGH		V_{IH}	6,55	–	–	V
Input current	V_I = 1 to 44 V	I_I	95	–	300	μA
Change of input current						
overdrive of other inputs $\Sigma(-I_I) < 10$ mA	$V_I < V_{CC} - 1$ V	ΔI_I	–	–	120	μA
	$V_I > V_{CC} - 1$ V	ΔI_I	–	–	158	μA
overdrive of other inputs $\Sigma(-I_I) < 90$ mA	$V_I < V_{CC} - 1$ V	ΔI_I	–	–	280	μA
	$V_I > V_{CC} - 1$ V	ΔI_I	–	–	320	μA
Input voltage by current overdrive	$\Sigma(-I_I)$ = 10 mA	V_I	46	–	65	V
Output voltage without clamping (pin 14 open)						
LOW	$I_{OL} \leqslant 0{,}095$ mA	V_{OL}	–	–	0,35	V
	I_{OL} = 0,095 to 1 mA	V_{OL}	–	–	1	V
	I_{OL} = 1 to 2,5 V	V_{OL}	–	–	1,5	V
HIGH	$-I_{OH} \leqslant 5$ mA	V_{OH}	$V_{CC}-1{,}5$	–	–	V
Output voltage with clamping (pin 14 at V_Z)	V_Z = 2,5 to V_{CC} – 1 V					
HIGH	I_{OH} = 0 mA	V_{OH}	(V_Z –0,5)	–	(V_Z + 0,245)	V
	I_{OH} = 1 mA	V_{OH}	(V_Z –0,5)	–	(V_Z + 0,15)	V
	I_{OH} = 3 mA	V_{OH}	(V_Z –0,5)	–	V_Z	V
	I_{OH} = 0 mA; V_Z = 0 V	V_{OH}	–	–	0,75	V
Output short-circuit current						
LOW-signal	output at V_{CC}	I_{OscL}	–	–	11	mA
HIGH-signal	output at V_{EE} (0 V)	$-I_{OscH}$	5	–	28,5	mA
HIGH-signal	output at V_{EE} (0 V); T_j = 140 °C	$-I_{OscH}$	–	–	10	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Current out of pin 14 (Z) when currents are forced into outputs	$-I_O \leqslant 3$ mA	$-I_Z$	–	–	2,2	mA
	$\Sigma I_O = (I_{O1} + I_{O2} + I_{O3})$	$-I_Z$	ΣI_O	–	–	mA
Current into pin 14 (Z) when inputs are set for output to be LOW	$-I_O = 30$ mA; $V_O \leqslant V_{EE}$	I_Z	–	–	300	μA
Supply current change	input and/or output voltages are negative with respect to V_{EE}	ΔI_{CCmax}	$(0{,}3 \times \lvert I_I \rvert) + (0{,}55 \times \lvert I_O \rvert)$			mA
Propagation delays						
gates 1 and 3						
HIGH to LOW		t_{PHL}	1	–	7	μs
LOW to HIGH		t_{PLH}	1	–	7	μs
gate 2						
HIGH to LOW	without capacitor	t_{PHL}	0,1	–	4	μs
LOW to HIGH	without capacitor	t_{PLH}	0,3	–	6	μs
HIGH to LOW	with capacitor; C in μF	t_{PHL}	38 x C	–	113 x C	μs
LOW to HIGH	with capacitor; C in μF	t_{PLH}	142 x C	–	334 x C	μs
Voltage spikes output LOW	see note 1	V_{OL}	–	–	2	V

Note to the characteristics

1. V_{CC} rising from 0 to 14 V; all inputs open; internally it is guaranteed that the input threshold voltage $V_{IL} > V_{OL}$.

APPLICATION INFORMATION

The following figures (Figs 4 to 11) give some examples of the basic industrial control functions.

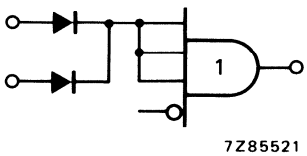


Fig. 4 OR function.

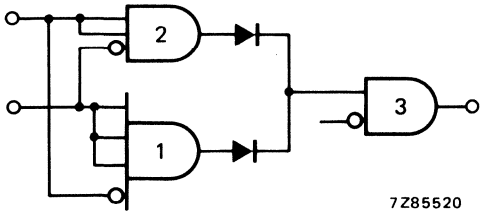


Fig. 5 EXCLUSIVE-OR function.

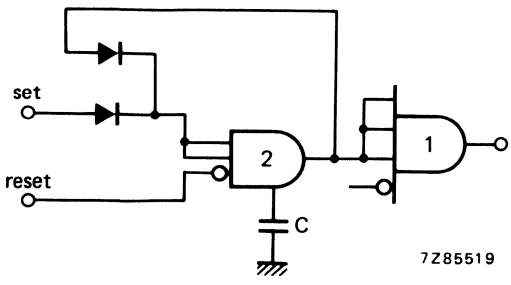


Fig. 6 Delayed memory; reset is dominating.

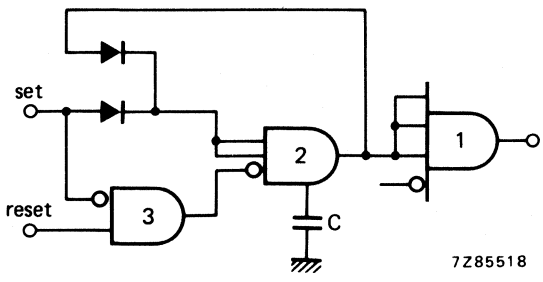


Fig. 7 Delayed memory; set is dominating.

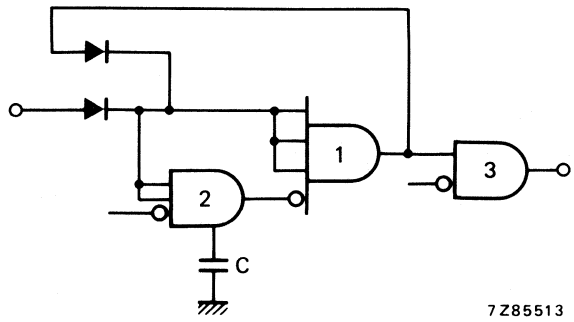


Fig. 8 Monostable flip-flop; for C = 4,7 μF, 1 s no reaction.

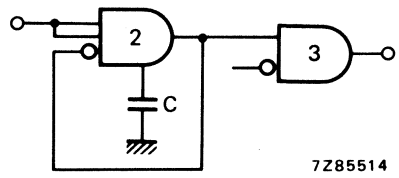


Fig. 9 Start delay function.

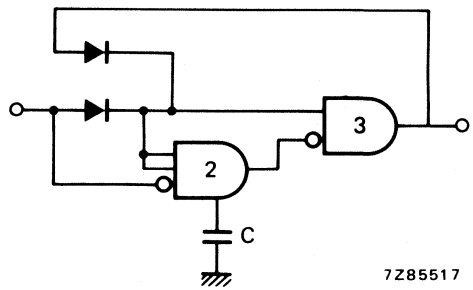


Fig. 10 Decay delay function.

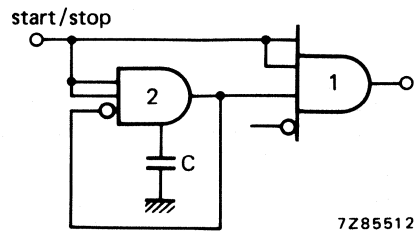


Fig. 11 Square-wave oscillator.

OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The TCA520 is a bipolar integrated operational amplifier primarily intended for low-power, low-voltage applications and as a comparator in digital systems.

Features

- Wide supply voltage range
- Low supply voltage operation
- Low power consumption
- Low input bias current
- Offset compensation facility
- Frequency compensation facility
- High slew rate
- Large output voltage swing
- TTL compatible output

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		2 to 20	V
Supply current	I_{CC}	typ.	0,8	mA
Input bias current	I_{IB}	typ.	60	nA
Output voltage range	V_O		0,1 to V_{CC}–0,1	V
D.C. differential voltage amplification	A_{VD}	typ.	15 000	
Slew rate	S_{VOAV}	typ.	25	V/μs
Operating ambient temperature range	T_{amb}		–25 to + 85	°C

PACKAGE OUTLINES

TCA520B : 8-lead DIL; plastic (SOT-97).
TCA520D: 8-lead mini-pack; plastic (SO-8; SOT-96A).

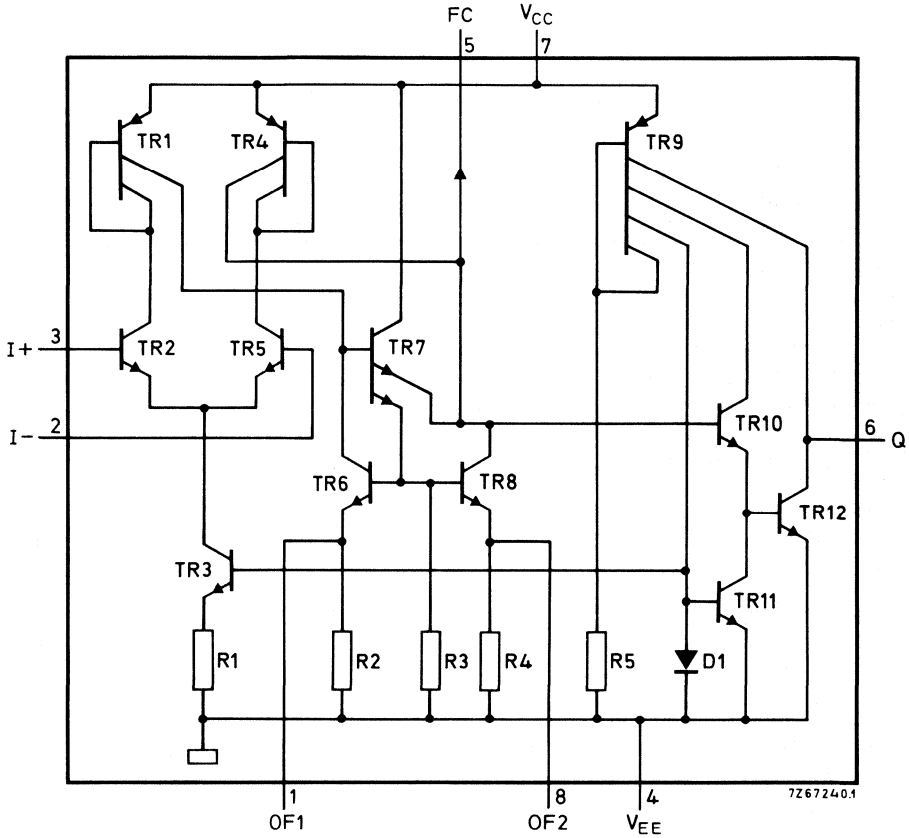


Fig. 1 Circuit diagram.

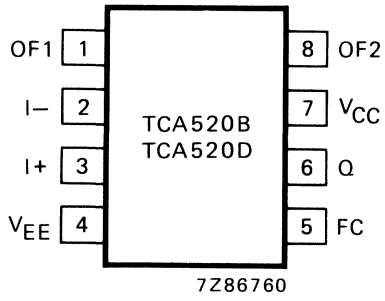


Fig. 2 Pinning diagram.

PINNING

1	OF1	offset compensation connection
2	I−	inverting input
3	I+	non-inverting input
4	V_{EE}	ground connection
5	FC	frequency compensation connection
6	Q	output
7	V_{CC}	positive supply connection
8	OF2	offset compensation connection

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	22	V
Input voltage	V_I	max.	V_{CC}	V
	$-V_I$	max.	0	V
Differential input voltage	$\pm V_{ID}$	max.	2	V
Power dissipation at T_{amb} = 85 °C	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−55 to + 125	°C
Operating ambient temperature range	T_{amb}		−25 to + 85	°C

CHARACTERISTICS

V_{CC} = 5 V; V_{EE} = 0 V; T_{amb} = 25 °C; R_L from Q to V_{CC} unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply V_{CC}; pin 7					
Supply current, unloaded	I_{CC}	0,5	0,8	1,2	mA
Inputs I+ and I−; pins 3 and 2					
Input voltage	V_I	0,9	–	V_{CC}−0,5	V
Input bias current	I_{IB}	–	60	250	nA
Input offset voltage	V_{IO}	–	1	6	mV
Variation with temperature	ΔV_{IO}	–	5	–	μV/K
Input offset current	I_{IO}	–	10	75	nA
Common-mode rejection ratio	k_{CMR}	70	100	–	dB
Input noise voltage at f = 1 kHz	$V_{n(rms)}$	–	15	–	nV/√Hz
Input noise current at f = 1 kHz	$I_{n(rms)}$	–	0,4	–	pA/√Hz
Input noise angular frequency	f_c	–	300	–	Hz
Output Q; pin 6					
Output voltage range at R_L = 5 kΩ	V_Q	0,1	–	V_{CC}−0,1	V
Output current					
HIGH at $V_Q = V_{CC} - 0{,}4$ V	$-I_{OH}$	100	200	–	μA
LOW at V_Q = 0,4 V	I_{OL}	6	12	–	mA
D.C. voltage amplification at R_L = 5 kΩ	A_{VD}	10 000	15 000	–	
A.C. voltage amplification at f = 1 kHz; C_{FC} = 100 pF	A_{vd}	–	58	–	dB
Slew rate (average rate of change of the output voltage) at R_L = 1 kΩ					
C_{FC} = 0 pF	S_{VOAV}	–	25	–	V/μs
C_{FC} = 100 pF	S_{VOAV}	–	500	–	mV/μs

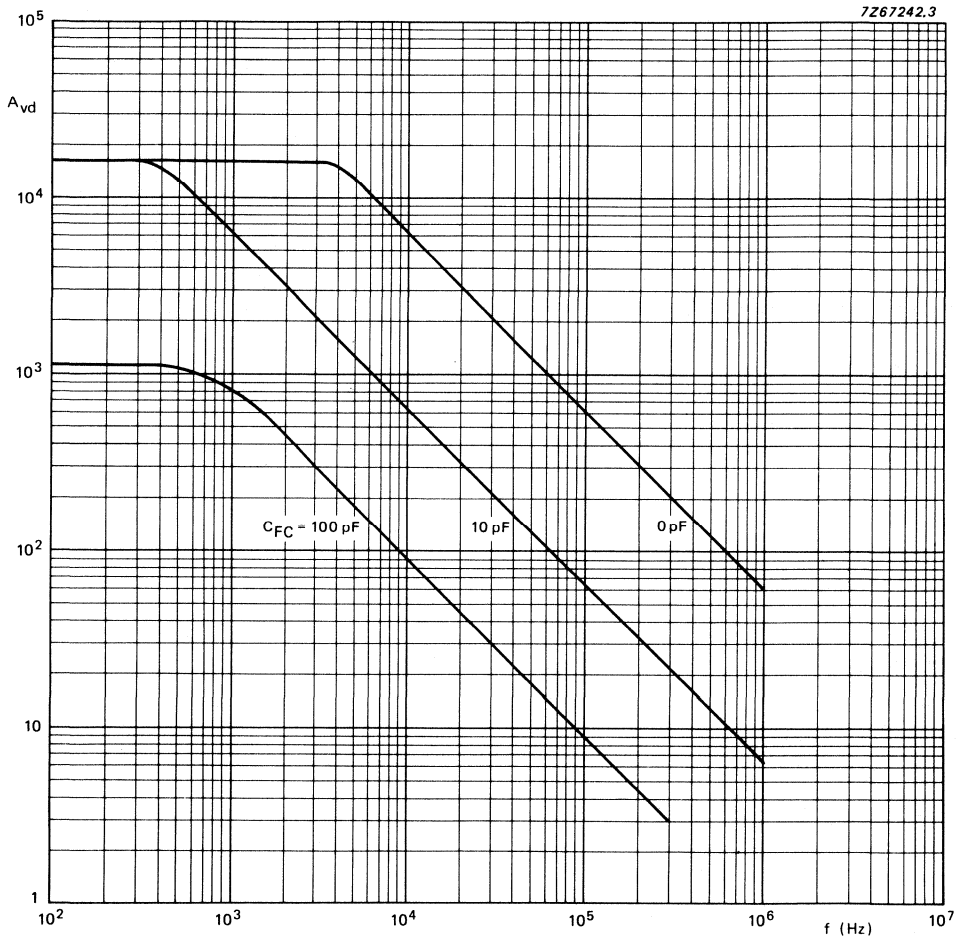


Fig. 3 Typical values of the open-loop voltage amplification as a function of frequency.

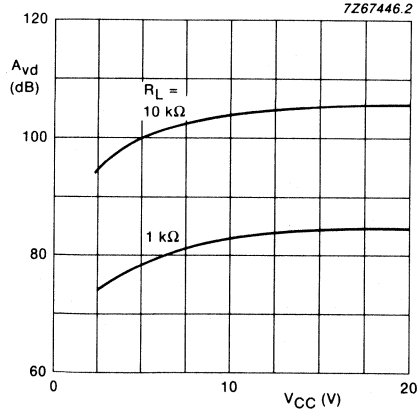


Fig. 4 Typical values of the open-loop voltage amplification as a function of supply voltage.

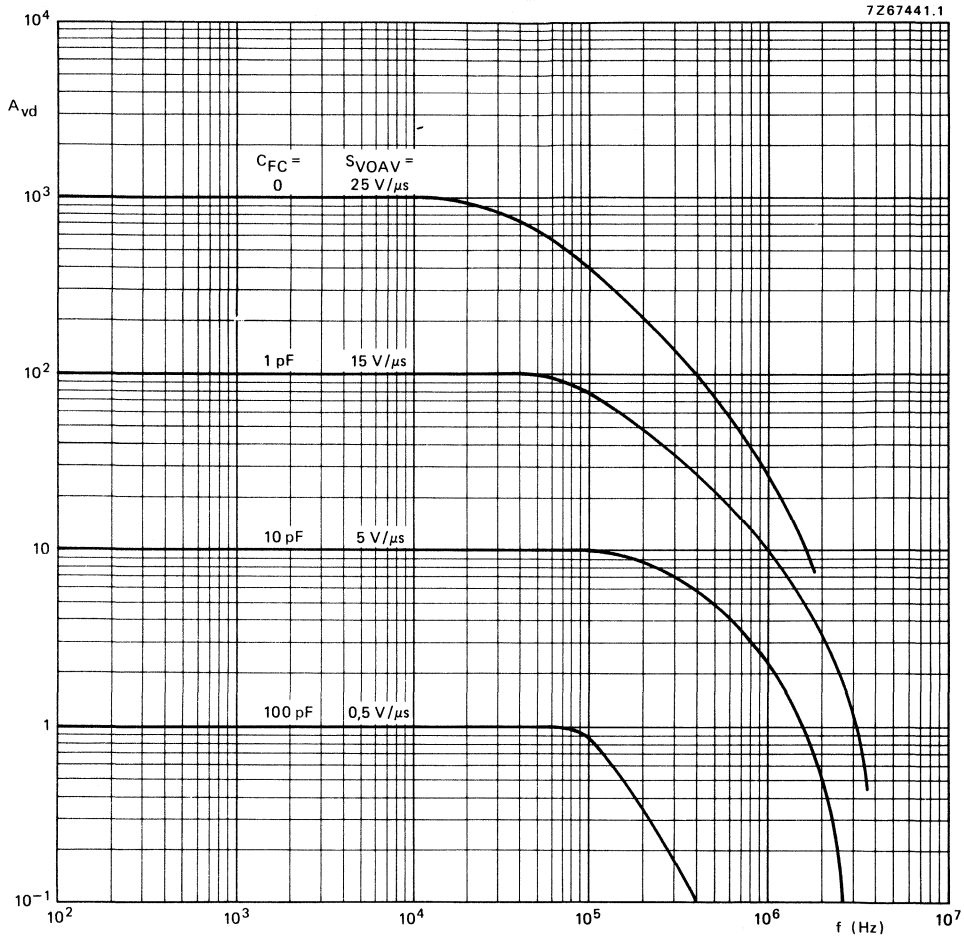


Fig. 5 Typical frequency response and slew rate for various closed-loop gains.

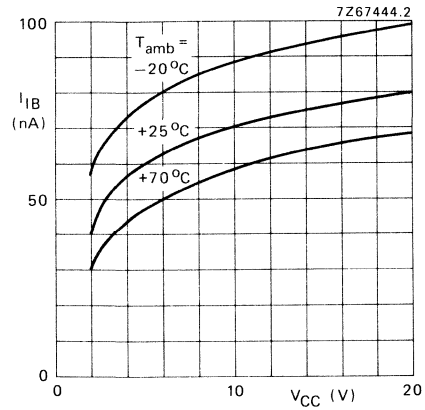


Fig. 6 Typical values of the input bias current as a function of supply voltage, with ambient temperature as a parameter.

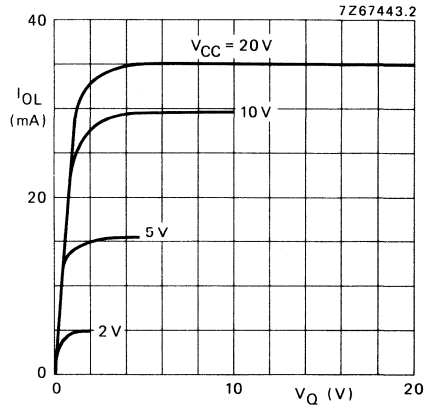


Fig.7 Typical output current LOW as a function of output voltage, with supply voltage as a parameter.

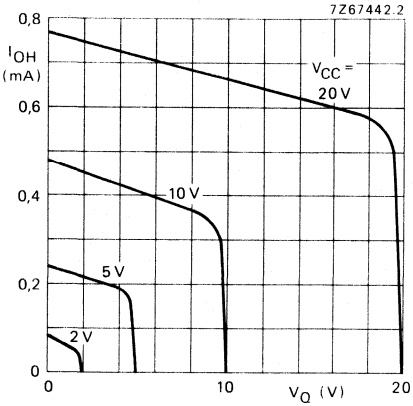


Fig.8 Typical output current HIGH as a function of ouput voltage, with supply voltage as a parameter.

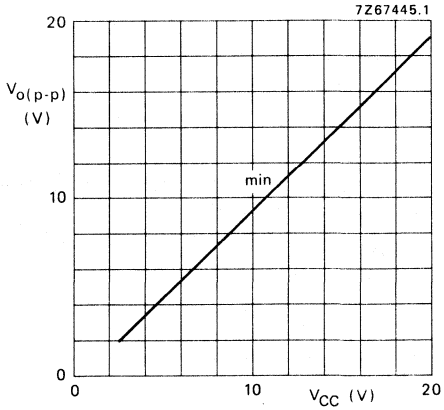


Fig. 9 Minimum values of the output voltage swing as a function of supply voltage for R_L = 1 kΩ.

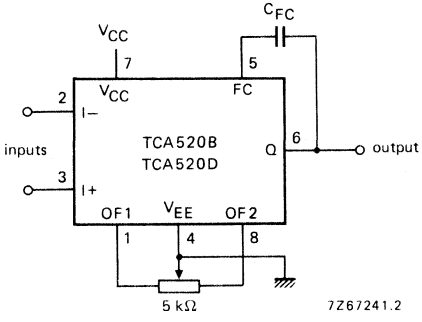


Fig. 10 Typical arrangement of the TCA520 with frequency and offset compensation.

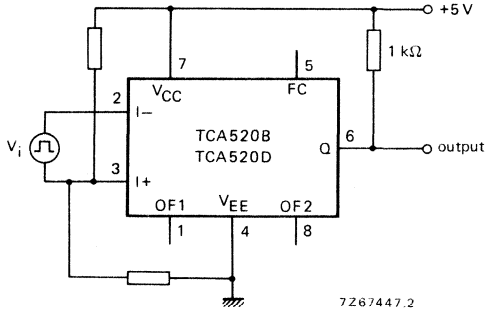


Fig. 11 Typical application of the TCA520 as a comparator; $|V_{2\text{-}3}|$ maximum 2 V.

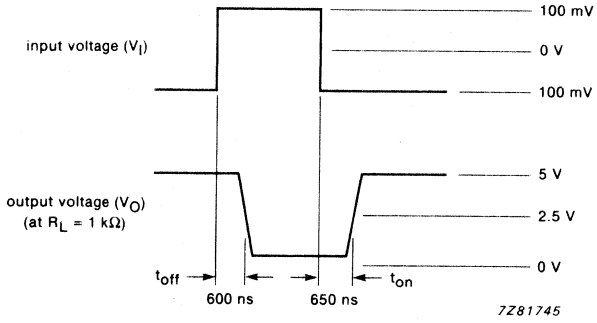


Fig. 12 Typical propagation delay time.

PROPORTIONAL-CONTROL TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperature control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Features

- Adjustable proportional range width
- Adjustable hysteresis
- Adjustable trigger pulse width
- Adjustable firing burst repetition time
- Control range translation facility
- Failsafe operation
- Supplied from the mains
- Provides supply for external temperature bridge

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13,7 V
Stabilized supply voltage for temperature bridge	V_Z	typ.	8 V
Supply current (average value)	$I_{16(AV)}$	typ.	10 mA
Trigger pulse width	t_w	typ.	200 μs
Firing burst repetition time at C_T = 68 μF	T_b	typ.	41 s
Output current	$-I_{OH}$*	max.	150 mA
Operating ambient temperature range	T_{amb}		−20 to + 75 °C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

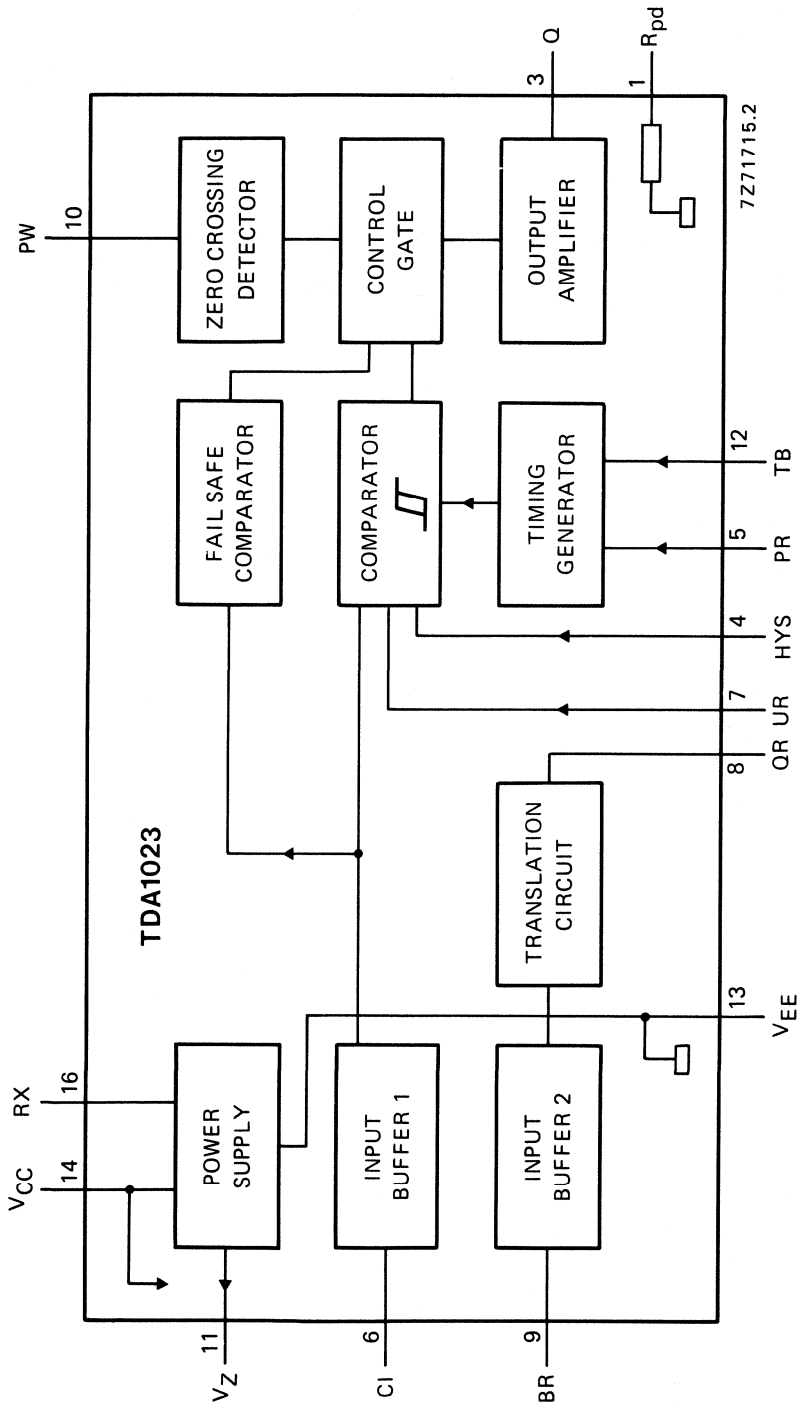


Fig. 1 Block diagram.

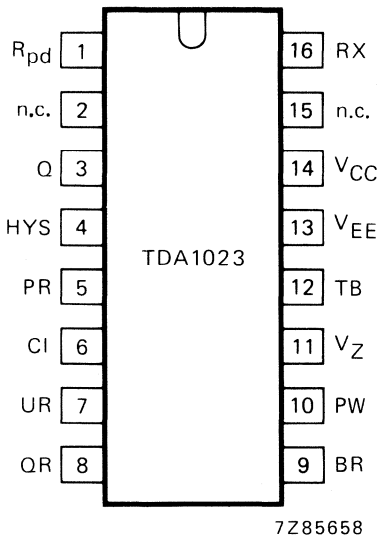


Fig. 2 Pinning diagram.

PINNING

1	R_{pd}	internal pull-down resistor connection
2	n.c.	not connected
3	Q	output
4	HYS	hysteresis control input
5	PR	proportional range control input
6	CI	Control input
7	UR	unbuffered reference input
8	QR	output of reference buffer
9	BR	buffered reference input
10	PW	pulse width control input
11	V_Z	reference supply output
12	TB	firing burst repetition time control input
13	V_{EE}	ground connection
14	V_{CC}	positive supply connection
15	n.c.	not connected
16	RX	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These trigger pulses coincide with the zero crossings of the mains voltage. This minimizes r.f. interference and transients on the mains supply. The trigger pulses come in bursts, with the net effect that the load is periodically switched on and off. This further minimizes mains pollution. The average power in the load is varied by varying the duration of the trigger pulse burst, in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_Z (pins 14, 16 and 11)

The TDA1023 is supplied from the a.c. mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is connected to the neutral line (see Fig. 4a). A smoothing capacitor C_S has to be connected between the V_{CC} and V_{EE} connections.

The circuit contains a string of stabilizer diodes between the RX and V_{EE} connections that limit the d.c. supply voltage, and a rectifier diode between the RX and V_{CC} connections (see Fig. 3).

At pin 11 the device provides a stabilized reference voltage V_Z for an external temperature sensing bridge.

The operation of the supply arrangement is as follows. During the positive half of the mains cycles the current through external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX reaches the stabilizing voltage of the internal stabilizer diodes. R_D should be chosen such that it can supply the current I_{CC} for the TDA1023 itself plus the average output current $I_{3(AV)}$ plus the current required from the V_Z connection for an external temperature bridge, and recharge the smoothing capacitor C_S (see Figs 9 to 12). Any excess current is bypassed by the internal stabilizer diodes. Note that the maximum rated supply current must not be exceeded.

During the negative half of the mains cycles external smoothing capacitor C_S has to supply the sum of the currents mentioned above. Its capacitance must be high enough to maintain the supply voltage above the minimum specified limit.

FUNCTIONAL DESCRIPTION (continued)

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig. 4b and 9 to 12).

A further reduction of dissipation is possible by using a high-quality voltage dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Asuitable VDR connected across the mains provides protection of the TDA1023 and of the triac against mains-borne transients.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For room temperature control (5 °C to 30 °C) the best performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input, and the output of the reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). In this arrangement the translation circuit ensures that most of the potentiometer rotation can be used to cover the room temperature range. This provides an accurate temperature setting and a linear temperature scale.

If the translation circuit is not required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12) and the buffered reference input BR (pin 9), which is inactive now, must be connected to the reference supply output V_Z (pin 11).

In all arrangements the train of output pulses becomes longer when the voltage at the control input CI (pin 6) becomes lower.

Proportional range control input PR (pin 5)

With the proportional range control input PR open the output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6). For temperature control this corresponds with a temperature difference of only 1 K.

This range may be increased to 400 mV, i.e. 5 K, by connecting the proportional range control input PR (pin 5) to ground. Intermediate values are obtained by connecting the PR input to ground via a resistor R5, see Table 1.

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0,25 K.

Hysteresis is increased to 320 mV, corresponding with 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 to ground via a resistor R4. See Table 1 for a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The trigger pulse width may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor R_S between the trigger pulse width control input PW (pin 10) and the a.c. mains. The pulse width is inversely proportional to the input current (see Fig. 13).

Output Q (pin 3)

Since the circuit has an open-emitter output, it is capable of sourcing current, i.e. supplying a current out of the output. Therefore it is especially suited for generating positive-going trigger pulses. The output is current-limited and protected against short-circuits. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

FUNCTIONAL DESCRIPTION (continued)

A gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8). This minimizes the total supply current and the power dissipation.

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1,5 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection), intended for use with sensitive triacs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage, d.c.	V_{CC}	max.	16 V
Supply current			
average	$I_{16(AV)}$	max.	30 mA
repetitive peak	$I_{16(RM)}$	max.	100 mA
non-repetitive peak	$I_{16(SM)}$	max.	2 A
Input voltage, all inputs	V_I	max.	16 V
Input current, CI, UR, BR, PW input	$I_{6;7;9;10}$	max.	10 mA
Voltage on R_{pd} connection	V_1	max.	16 V
Output voltage, Q, QR, V_Z output	$V_{3;8;11}$	max.	16 V
Output current			
average	$-I_{OH(AV)}$	max.	30 mA
peak, max. 300 μs	$-I_{OH(M)}$	max.	700 mA
Total power dissipation	P_{tot}	max.	500 mW
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−20 to + 75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = −20 to + 75 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply: V_{CC} and RX (pins 14 and 16)					
Internally stabilized supply voltage at I_{16} = 10 mA	V_{CC}	12	13,7	15	V
Variation with I_{16}	$\Delta V_{CC}/\Delta I_{16}$	–	30	–	mV/mA
Supply current at V_{16-13} = 11 to 16 V; I_{10} = 1 mA; f = 50 Hz; pin 11 open; $V_{6-13} > V_{7-13}$; pins 4 and 5 open	I_{16}	–	–	6	mA
pins 4 and 5 grounded	I_{16}	–	–	7,1	mA
Reference supply output V_Z (pin 11) for external temperature bridge					
Output voltage	V_{11-13}	–	8	–	V
Output current	$-I_{11}$	–	–	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)					
Input voltage to inhibit the output	V_{6-13}	–	7,6	–	V
Input current at V_I = 4 V	$I_{6;7;9}$	–	–	2	μA
Hysteresis control input HYS (pin 4)					
Hysteresis, pin 4 open	ΔV_6	9	20	40	mV
pin 4 grounded	ΔV_6	–	320	–	mV
Proportional range control input PR (pin 5)					
Proportional range, pin 5 open	ΔV_6	50	80	130	mV
pin 5 grounded	ΔV_6	–	400	–	mV
Pulse width control input PW (pin 10)					
Pulse width at $I_{10(RMS)}$ = 1 mA; f = 50 Hz	t_w	100	200	300	μs
Firing burst repetition time control input TB (pin 12)					
Firing burst repetition time, ratio to capacitor C_T	T_b/C_T	320	600	960	ms/μF
Output of reference buffer QR (pin 8)					
Output voltage at input voltage V_{9-13} = 1,6 V	V_{8-13}	–	3,2	–	V
V_{9-13} = 4,8 V	V_{8-13}	–	4,8	–	V
V_{9-13} = 8 V	V_{8-13}	–	6,4	–	V

	symbol	min.	typ.	max.	unit
Output Q (pin 3)					
Output voltage HIGH at $-I_{OH}$ = 150 mA	V_{OH}	10	–	–	V
Output current HIGH	$-I_{OH}$	–	–	150	mA
Internal pull-down resistor R_{pd} (pin 1)					
Resistance to V_{EE}	R_{pd}	1	1,5	3	kΩ

Table 1 Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	proportional range resistor R5 kΩ	minimum hysteresis mV	maximum hysteresis resistor R4 kΩ
80	open	20	open
160	3,3	40	9,1
240	1,1	60	4,3
320	0,43	80	2,7
400	0	100	1,8

Table 2 Timing capacitor C_T values.

effective d.c. value	marked a.c. specification		catalogue number*
μF	μF	V	
68	47	25	2222 016 90129
47	33	40	– – 90131
33	22	25	– 015 90102
22	15	40	– – 90101
15	10	25	– – 90099
10	6,8	40	– – 90098

* Special electrolytic capacitors recommended for use with TDA1023.

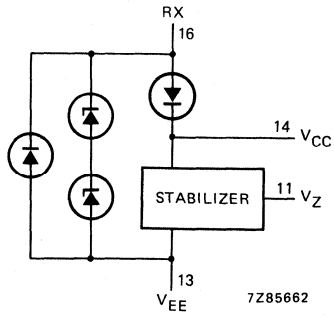


Fig. 3 Internal supply connections.

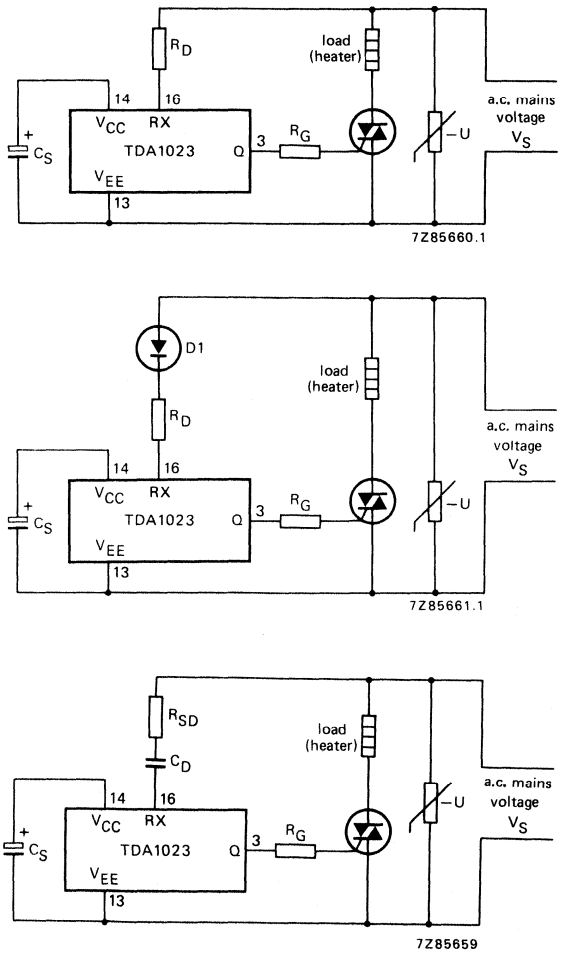


Fig. 4 Alternative supply arrangements.

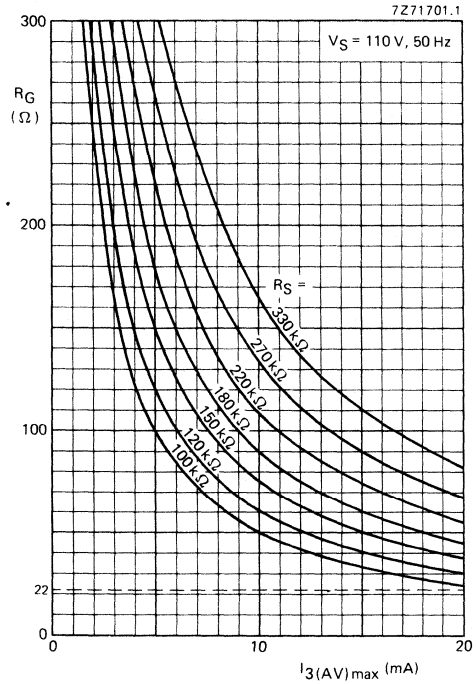


Fig. 5.

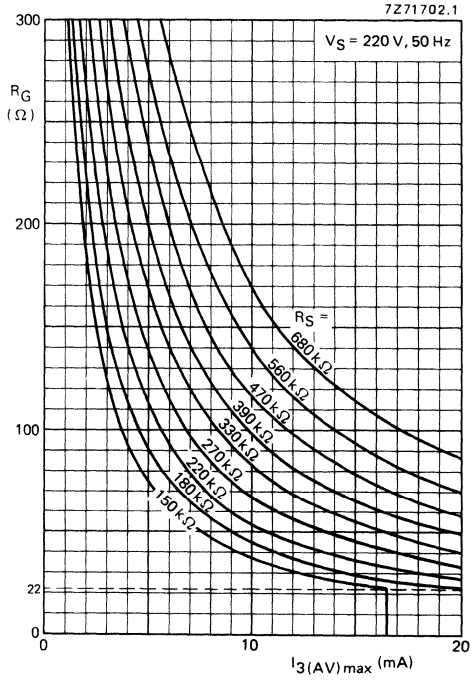


Fig. 6.

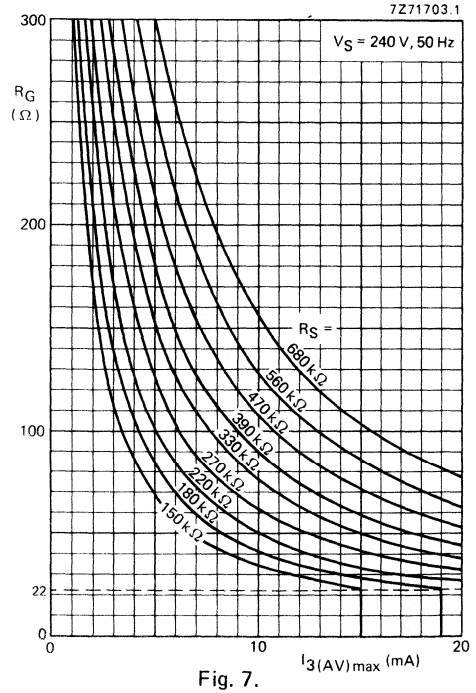


Fig. 7.

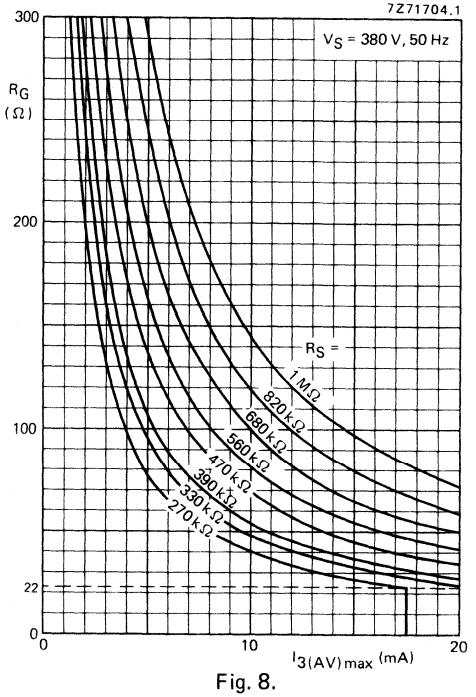


Fig. 8.

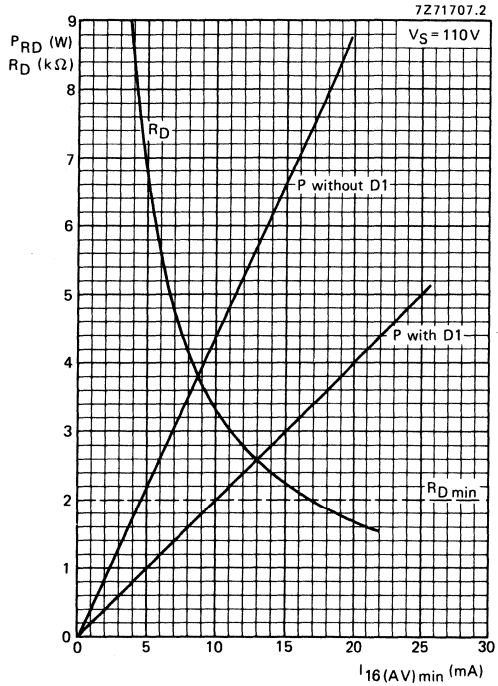


Fig. 9.

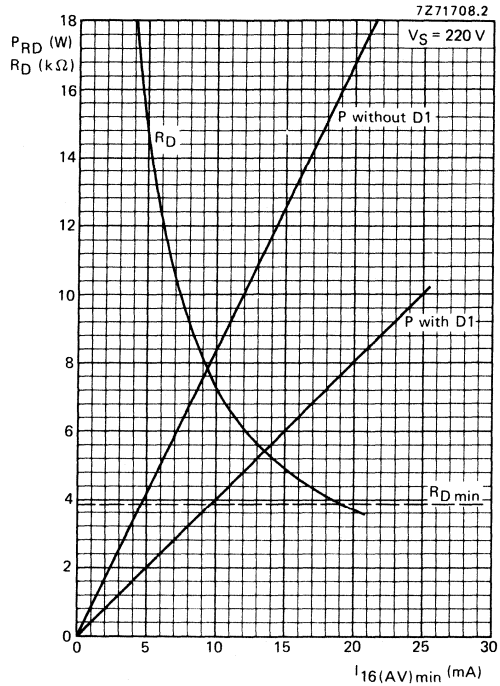


Fig. 10.

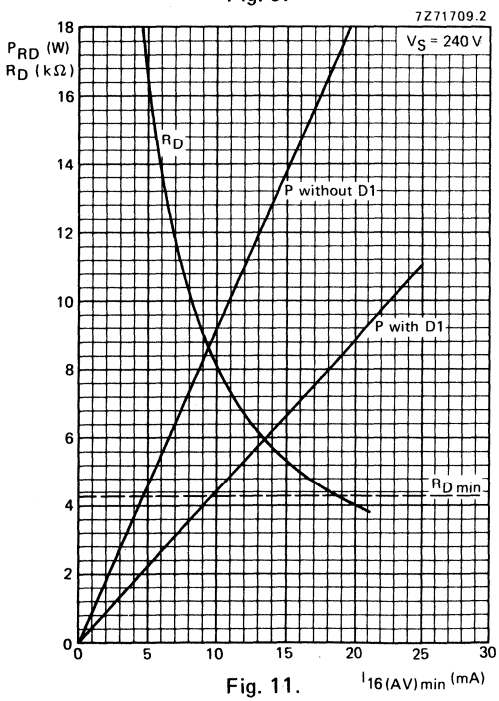


Fig. 11.

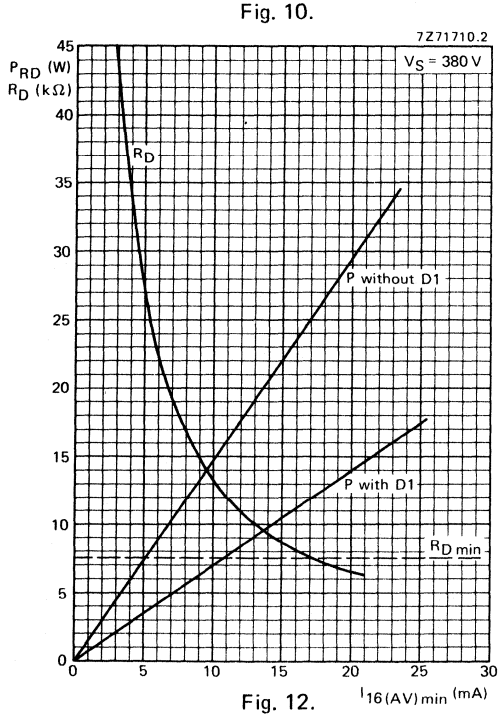


Fig. 12.

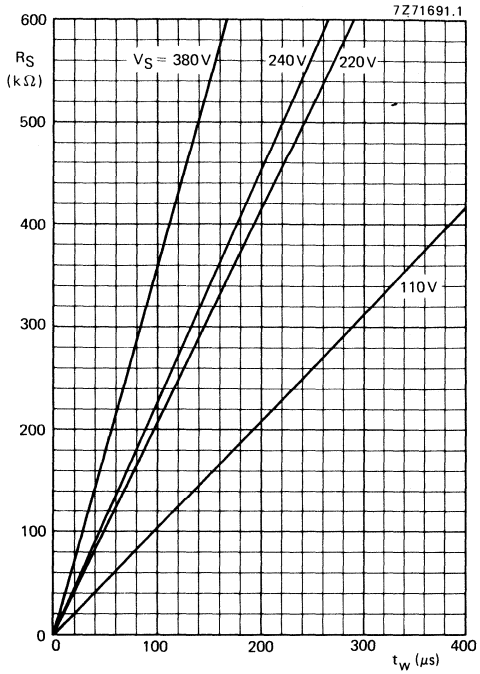


Fig. 13 Synchronization resistor R_S as a function of required trigger pulse width t_w with mains voltage V_S as a parameter.

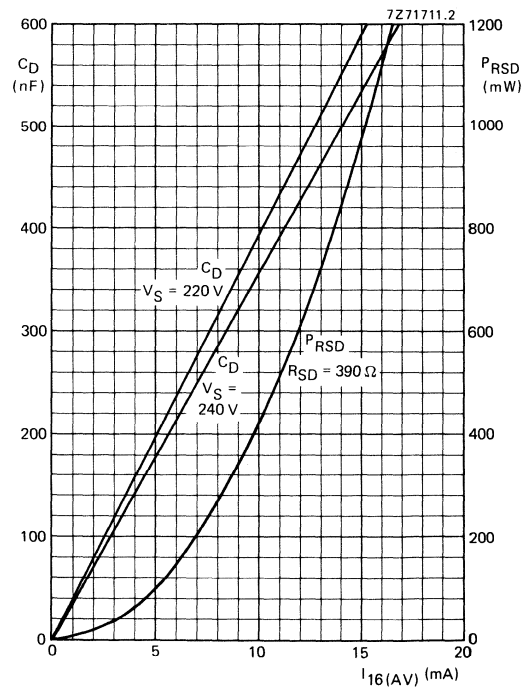


Fig. 14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in voltage dropping resistor R_{SD} as a function of the average supply current $I_{16(AV)}$ with the mains supply voltage V_S as a parameter.

APPLICATION INFORMATION

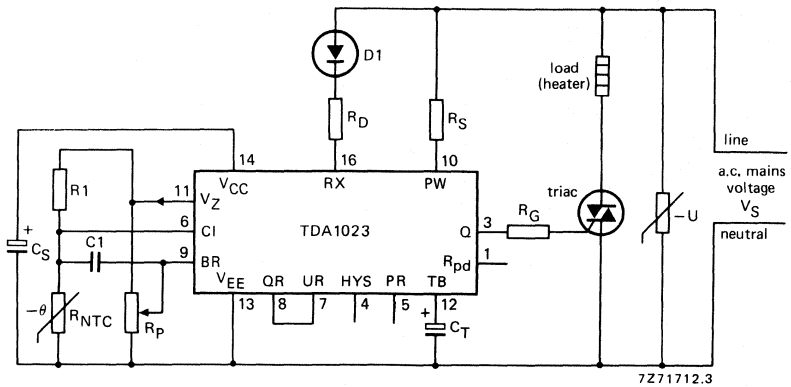


Fig. 15 The TDA1023 used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Conditions

Mains supply: V_S = 220 V

Temperature range = 5 to 30 °C

BT139 data: $V_{GT} < 1{,}5$ V; $I_{GT} > 70$ mA; $I_L < 60$ mA } at T_j = 25 °C

Table 3 Temperature controller component values (see Fig. 15).

parameter	symbol	value	remarks
Trigger pulse width	t_w	75 μs	see BT139 data sheet
Synchronization resistor	R_S	180 kΩ	see Fig. 13
Gate resistor	R_G	110 Ω	see Fig. 6
Max. average gate current	$I_{3(AV)}$	4,1 mA	see Fig. 8
Hysteresis resistor	R4	n.c.	see Table 1
Proportional band resistor	R5	n.c.	see Table 1
Min. required supply current	$I_{16(AV)}$	11,1 mA	
Mains dropping resistor	R_D	6,2 kΩ	see Fig. 10
Power dissipated in R_D	P_{RD}	4,6 W	see Fig. 10
Timing capacitor (eff. value)	C_T	68 μF	see Table 2
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 593 62512
Rectifier diode	D1	BYW56	
Resistor to pin 11	R1	18,7 kΩ	1% tolerance
NTC thermistor (at 25 °C)	R_{NTC}	22 kΩ	B = 4200 K cat. no. 2322 642 12223
Potentiometer	R_P	22 kΩ	
Capacitor between pins 6 and 9	C1	47 nF	
Smoothing capacitor	C_S	220 μF; 16 V	
If R_D and D1 are replaced by C_D and R_{SD}			
Mains dropping capacitor	C_D	470 nF	
Series dropping resistor	R_{SD}	390 Ω	see Fig. 14
Power dissipated in R_{SD}	P_{RSD}	0,6 W	
Voltage dependent resistor	VDR	250 V a.c.	cat. no. 2322 594 62512

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_P to pin 7; pin 8 open; pin 9 connected to pin 11.

APPLICATION INFORMATION SUPPLIED ON REQUEST

CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TDA1060 is a bipolar integrated circuit intended for the control of a switched-mode power supply. It incorporates all the control functions likely to be required in switched-mode power supplies for professional equipment.

Features

- Suitability for a wide range of supply voltages
- Built-in stabilized power supply for external circuitry
- Built-in temperature-compensated voltage reference
- Adjustable frequency
- Adjustable control loop sensitivity
- Adjustable pulse width
- Adjustable maximum duty factor
- Adjustable overcurrent protection limit
- Low supply voltage protection with hysteresis
- Loop fault protection
- Slow-start facility
- Feed-forward facility
- Core saturation protection facility
- Overvoltage protection facility
- Remote ON/OFF switching facility

QUICK REFERENCE DATA

Supply voltage (voltage source)	V_{CC}	max.	18 V
Supply current (current source)	I_{CC}	max.	30 mA
Output current	$-I_{14}; I_{15}$	max.	40 mA
Stabilized voltage	V_Z	typ.	8,4 V
Reference voltage	V_{ref}	typ.	3,72 V
Output pulse repetition frequency range	f_o	50 Hz to 100	kHz
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C

PACKAGE OUTLINES

TDA1060, TDA1060A: 16-lead DIL; plastic (SOT-38).
TDA1060B: 16-lead DIL ceramic (cerdip) (SOT-74).
TDA1060T: 16-lead mini-pack; plastic (SO-16; SOT-109A).

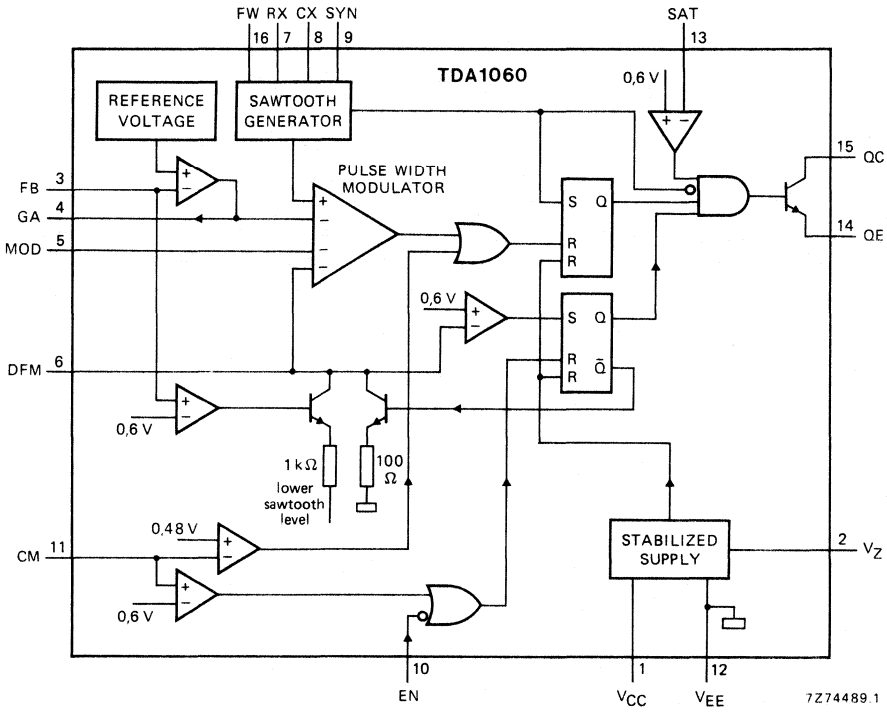


Fig. 1 Block diagram.

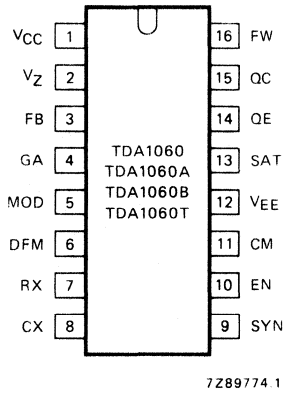


Fig. 2 Pinning diagram.

PINNING

1	V_{CC}	positive supply connection
2	V_Z	stabilized voltage output
3	FB	feedback input
4	GA	gain adjustment output
5	MOD	modulation input
6	DFM	maximum duty factor input
7	RX	external resistor connection
8	CX	external capacitor connection
9	SYN	synchronization input
10	EN	ENABLE input
11	CM	overcurrent protection input
12	V_{EE}	common
13	SAT	core saturation and overvoltage protection input
14	QE	emitter output
15	Q_C	collector output
16	FW	feed-forward input

FUNCTIONAL DESCRIPTION

The TDA1060 contains the control loop for a fixed-frequency pulse-duration regulated SMPS. The device works as follows. The output voltage V_O of the SMPS is sensed via a feedback network and compared with an internal reference voltage V_{ref}. Any difference between V_O and V_{ref} is amplified and fed to a pulse-width modulator (PWM), where it is compared with the instantaneous level of a ramp waveform (sawtooth) from an oscillator. The output from the PWM is a rectangular waveform synchronized with the oscillator waveform; its duty factor depends on the difference between V_O and V_{ref}. This signal drives the base of the SMPS power switching transistor so that its conduction period and hence the amount of energy transferred from the input to the output of the SMPS is controlled, resulting in a constant output voltage.

Stabilized power supply: V_{CC} and V_Z (pins 1 and 2)

The circuit contains a voltage/current regulator and may be supplied either by a current source (e.g. a series resistor connected to the high voltage input of the SMPS), or a voltage source (e.g. a 12 V battery).

The stabilized voltage, typically 8,4 V, is also available at V_Z, pin 2 for supplying external circuitry, e.g. a potentiometer to adjust the maximum duty factor. This supply output is protected against short-circuits. The current drawn from this output increases the total IC supply current by the same amount.

When the supply voltage V_{CC} becomes too low, i.e. $V_{CC} < V_Z + 0{,}2$ V, the circuit is automatically switched off. As soon as the supply voltage exceeds this threshold value by more than 0,2 V the circuit starts the SMPS via the slow start procedure.

Operating frequency: RX and CX (pins 7 and 8)

The frequency of the sawtooth generator, and hence of the output pulses, is set by an external resistor R7 at RX, pin 7, and an external capacitor C8 at CX, pin 8 (see Fig. 7). The frequency may be set between 50 Hz and 100 kHz and is virtually independent of the supply voltage.

Maximum duty factor and slow start: DFM (pin 6)

The maximum duty factor is set by the voltage on the duty factor input DFM (see Fig. 4). This voltage usually is derived from the stabilized power supply V_Z, pin 2, by an external voltage divider, see Fig. 8. As the upper and lower levels of the sawtooth waveform are set by an internal voltage divider, the accuracy of the maximum duty factor setting is determined by resistor ratios rather than by absolute values.

In case of a short-circuited feedback loop ($V_{3\text{-}12}$ less than typ. 600 mV) the duty factor input is internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ. The maximum duty factor permitted in that case sets a maximum limit to the impedance level of the external voltage divider at pin 6.

During the flyback of the sawtooth the output pulse is inhibited. For a 1 nF capacitor C8 at pin 8 this flyback time is 1 μs. This sets a natural limit to the duty factor.

The time constant for the slow start is determined by an external capacitor connected between the maximum duty factor input DFM and V_{EE}, pin 12, together with the impedance of the voltage divider at pin 6. This capacitor also determines the dead time before the slow start procedure for remote ON/OFF or when the current sensing voltage has exceeded 600 mV, see below.

If the DFM input is note used it should be connected to V_Z via a resistor of 5 kΩ.

FUNCTIONAL DESCRIPTION (continued)

Control loop sensitivity, stability, and feedback loop fault protection, FB and GA (pins 3 and 4)

The device contains a control loop error amplifier, i.e. a differential amplifier that compares the voltage on the feedback input FB, pin 3, with the internal reference voltage. This reference voltage is a temperature-compensated voltage source based on the band-gap energy of silicon.

The control loop sensitivity is determined by the closed-loop gain A_f of the error amplifier. Normally the output from the SMPS is connected to the feedback input FB via a voltage divider and a series resistor. The closed-loop gain of the error amplifier is set by applying feedback from the gain adjustment output GA, pin 4, to the feedback input FB by a resistor R3-4, see Fig. 8.

To avoid instability a capacitor should be connected between the gain output GA and V_{EE}, pin 12. A 22 nF capacitor will cause the frequency response to fall off above 600 Hz.

The feedback input FB is internally biased to the HIGH level, this gives a protection against a feedback loop fault: an open feedback loop will make the duty factor zero.

A shorted feedback loop (feedback voltage less than typ. 600 mV) causes the maximum duty factor input DFM to be internally biased to the lower level of the sawtooth waveform via a resistor of typ. 1 kΩ, thus substantially reducing the maximum duty factor. This duty factor will then be determined by the impedance of the external voltage divider at DFM, pin 6, and the internal biasing resistor.

Overcurrent protection input CM (pin 11)

There are two current limits, corresponding with voltages on the overcurrent protection input CM of typ. 480 mV and 600 mV. As soon as the voltage on this input exceeds 480 mV, the running output pulse is immediately terminated; the next pulse starts normally at the next period. If the voltage exceeds 600 mV, the output pulses are inhibited for a certain dead time, during which the slow start capacitor at pin 6 is unloaded. After this the circuit starts again with the slow start procedure.

If the overcurrent protection input CM is not used, it should be connected to V_{EE}, pin 12.

Feed-forward input FW (pin 16)

The feed-forward input FW can be connected to an external voltage divider from the input voltage of the SMPS, see Fig. 8. It has the effect of varying the supply voltage of the sawtooth generator with respect to the stabilized voltage. When the voltage on the feed-forward input increases, the upper level of the sawtooth is also increased. Since neither the voltage level that sets the maximum duty factor nor the feedback voltage are influenced by the feed-forward, the duty factor reduces (see Fig. 6). This can therefore compensate for mains voltage variations.

If feed-forward is not required the feed-forward input FW should be connected to V_{EE}, pin 12.

Synchronization input SYN (pin 9)

The frequency of the sawtooth waveform, and hence of the output pulses, can be synchronized via the TTL compatible synchronization input SYN. The synchronizing frequency must be lower than the oscillator free-running frequency. When the synchronization input is LOW the sawtooth generator is stopped; it starts again when the input goes HIGH. Synchronization pulses do not influence the slope of the sawtooth, and hence not the width of the output pulses, they only change their separation in time.

For free-running operation it is advisable to connect the synchronization input SYN to V_Z, pin 2.

Core saturation and overvoltage protection input SAT (pin 13)

To obtain a protection against core saturation, especially during transient conditions, the output transformer of the SMPS has to be fitted with a winding serving as a current sensor. Its output voltage is rectified and fed to the SAT input.

This core saturation protection may be combined with an overvoltage protection. To this end a portion of the SMPS output voltage is also fed to the SAT input either via a voltage divider or via a suitable regulator diode (zener diode). The output pulses are inhibited as long as the voltage on this input exceeds the threshold voltage, typ. 600 mV.

The voltage at the SAT input does not influence the frequency of the sawtooth generator and hence not of the output pulses.

If none of these protection facilities are used, the SAT input should be connected to V_{EE}, pin 12.

Remote ON/OFF switching: ENABLE input EN (pin 10)

The output pulses can be switched on and off by applying logic levels to the TTL compatible ENABLE input. A LOW level causes immediate inhibition of the output pulses, a subsequent HIGH level switches the circuit on with the slow-start procedure.

If this facility is not required, EN should be connected to V_Z, pin 2.

Modulation input MOD (pin 5)

The duty factor of the output pulses may be reduced below the value resulting from the voltages on the maximum duty factor input DFM and the gain adjust output GA by applying a lower voltage to the modulation input MOD. This input may be used with an external control loop, e.g. for constant-current control, or to obtain a fold-back characteristic.

If the modulation input is not used, it should be connected to V_Z, pin 2.

Output QC and QE (pins 13 and 14)

To avoid double pulses that might occur at an excessively low mains voltage or an excessively high output current the output is preceded by a latch. The two outputs offer a choice of output current polarity, QC giving a positive current, i.e. a current flowing into the output, and QE giving a negative current, a current flowing out of the output. The two connections have the additional advantage that the relatively large output currents do not flow through the V_{CC} and V_{EE} connections, where they could induce noise.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (voltage source)	V_{CC}	−0,5 to + 18	V
Supply current (current source)	I_{CC}	max. 30	mA
Feed-forward input voltage range			
$V_{CC} < 24$ V	V_{16-12}	0 to V_{CC}	V
$V_{CC} > 24$ V	V_{16-12}	0 to 24	V
Input voltage range (all other inputs)	V_I	0 to V_Z	V
Emitter output voltage range	V_{14-12}	0 to 5	V
Collector output voltage range	V_{15-12}	0 to V_{CC}	V
Output current			
d.c. (see Figs 3a, c and e)	$-I_{14}; I_{15}$	max. 40	mA
peak; t = max. 1 μs; duty factor d < 10%	$-I_{14}; I_{15}$	max. 200	mA
Storage temperature range			
TDA1060; T	T_{stg}	−55 to + 150	°C
TDA1060A	T_{stg}	−55 to + 150	°C
TDA1060B	T_{stg}	−55 to + 150	°C
Operating ambient temperature range			
TDA1060; T	T_{amb}	−25 to + 125	°C
TDA1060A	T_{amb}	0 to + 70	°C
TDA1060B	T_{amb}	−55 to + 150	°C
Power dissipation (see Figs 3b, d and f)	P_{tot}	max. 1	W

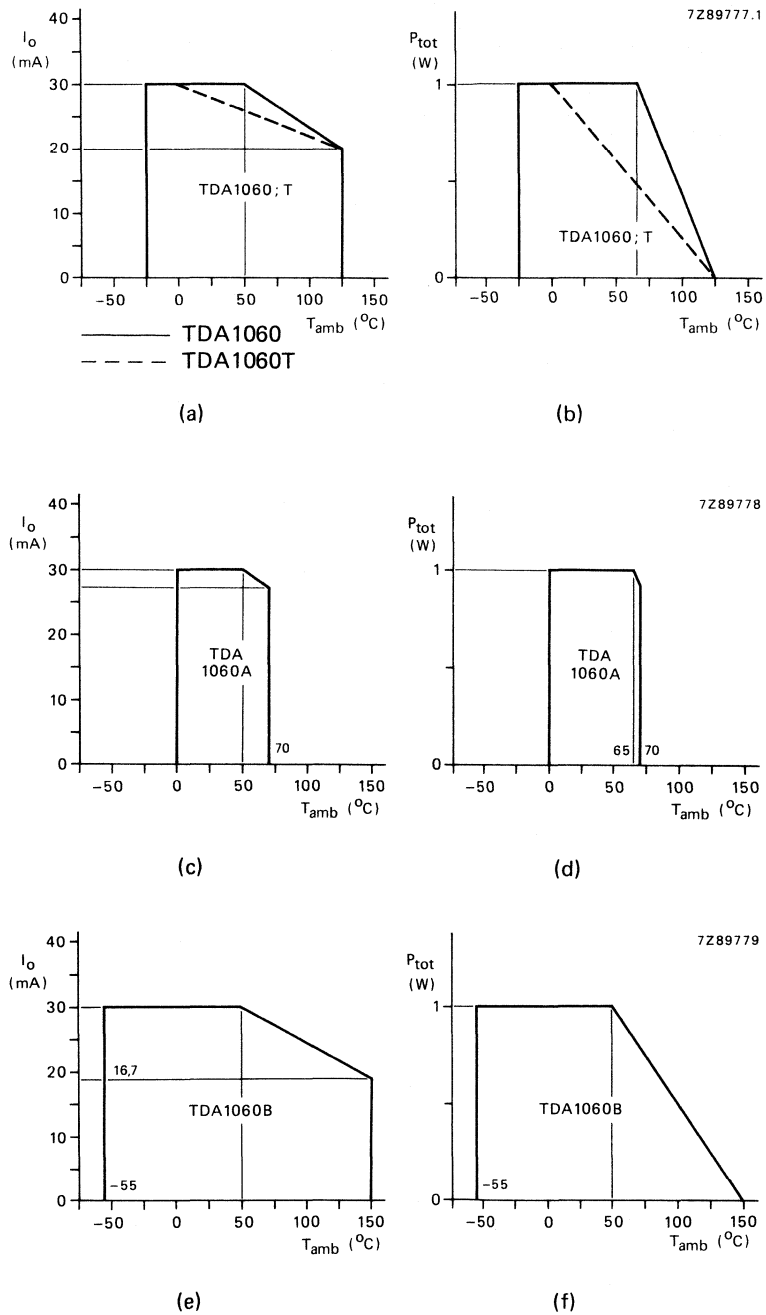


Fig. 3 Output current and power dissipation derating curves.

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = operating ambient temperature range, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Operating ambient temperature range					
TDA1060; T	T_{amb}	−25	–	125	°C
TDA1060A	T_{amb}	0	–	70	°C
TDA1060B	T_{amb}	−55	–	150	°C
Supply V_{CC} (pin 1)					
Supply voltage at I_{CC} = 15 mA					
TDA1060; T	V_{CC}	18,5	23	27	V
TDA1060A	V_{CC}	18,5	23	27	V
TDA1060B	V_{CC}	18	23	27,5	V
at I_{CC} = 30 mA					
TDA1060; T	V_{CC}	19,5	24	29	V
TDA1060A	V_{CC}	19,5	24	29	V
TDA1060B	V_{CC}	19	24	29,5	V
Supply current; R7 = 25 kΩ; duty factor δ = 50%; I_Z = 0; at T_{amb} = 25 °C	I_{CC}	2,5	–	10	mA
over ambient temperature range	I_{CC}	2,5	–	15	mA
Threshold voltage of low supply voltage protection at T_{amb} = 25 °C	V_{CC}	8,85	–	10,8	V
Variation with temperature	$-\Delta V_{CC}/\Delta T$	–	7,5	–	mV/K
Hysteresis of low supply voltage protection	ΔV_{CC}	–	500	–	mV
Stabilized supply output V_Z (pin 2)					
Output voltage at T_{amb} = 25 °C	V_Z	7,5	8,4	9	V
Variation with temperature	$\Delta V_Z/\Delta T$	−1,5	–	+ 1,5	mV/K
Output current	$-I_Z$	–	–	5	mA
Feedback input FB (pin 3)					
Input voltage, feedback operation	$V_{3\text{-}12}$	2	–	V_Z-1	V
Input current at $V_{3\text{-}12}$ = 2 V	$-I_3$	1,5	12	35	μA
Internal reference voltage, measured at pin 3; pins 3 and 4 interconnected and grounded via a 100 nF capacitor; T_{amb} = 25 °C	V_{ref}	3,42	3,72	4,03	V
Variation with temperature	$\frac{\Delta V_{ref}/V_{ref}}{\Delta T}$	–	0,01	–	%/K
Variation with supply voltage	$\frac{\Delta V_{ref}}{\Delta V_{CC}}$	–	0,8	–	mV/V

parameter	symbol	min.	typ.	max.	unit
Long-term variation with time	$\pm \Delta V_{ref}/\Delta t$	–	2	–	μV/h
Threshold voltage of feedback loop short-circuit protection at $T_{amb} = 25\,^{o}C$	$V_{3\text{-}12}$	470	600	720	mV
Variation with temperature	$\frac{\Delta V_{3\text{-}12}/V_{3\text{-}12}}{\Delta T}$	–	0,01	–	%/K
Gain adjustment output GA (pin 4)					
Open-loop gain, pin 3 to pin 4	A_o	–	60	–	dB
External feedback resistance	$R_{3\text{-}4}$	10	–	–	kΩ
Modulator input MOD (pin 5)					
Input current at $V_{5\text{-}12} = 2$ V; $V_{4;\,6\text{-}12} > 2$ V	$-I_5$	–	–	5	μA
Maximum duty factor input DFM (pin 6)					
Input voltage for limiting the duty factor to 50%; $f_o = 20$ to 50 kHz; $V_{16\text{-}12} = 0$ V	$V_{6\text{-}12}$	–	$0{,}42V_Z$	–	V
Input current at $V_{6\text{-}12} = 2$ V	$-I_6$	–	–	6	μA
Capacitor discharge current during fault condition	I_6	2,5	–	–	mA
Minimum output OFF time at C7 = 1,8 nF	t_{off}	–	1	–	μs
Variation of max. duty factor with temperature at $f_o = 20$ kHz and $\delta_{max} = 50\%$	$\Delta\delta_{max}/\Delta T$	–	0,02	–	%/K
Internal biasing resistor to V_{EE} at $V_{3\text{-}12} = 0$ V	$R_{6\text{-}12}$	0,75	1	1,25	kΩ
Synchronization input SYN (pin 9)					
Input voltage, sawtooth ON	V_{IH}	2	–	V_Z	V
sawtooth OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{9\text{-}12} = 0$ V	$-I_{IL}$	20	–	120	μA
External resistor connection RX (pin 7)					
External frequency adjustment resistor	R7	5	–	40	kΩ
External capacitor connection CX (pin 8)					
Sawtooth, upper level at $V_{16\text{-}12} = 0$ V	$V_{8\text{-}12}$	–	5,7	–	V
lower level	$V_{8\text{-}12}$	–	1,3	–	V
Oscillator frequency R7 = 6,4 kΩ, C8 = 6,4 nF	f_{osc}	–	30,5	–	kHz
Output pulse repetition frequency range	f_o	0,05	–	100	kHz
Variation with temperature	$\frac{\Delta f_o/f_o}{\Delta T}$	–	0,03	–	%/K

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Feed-forward input FW (pin 16)					
Input voltage					
for $V_{CC} < 24$ V	V_{16-12}	0	–	V_{CC}	V
for $V_{CC} > 24$ V	V_{16-12}	0	–	24	V
Input current at $V_{16-12} = 16$ V; $V_{CC} = 18$ V; $T_{amb} = 25$ °C	I_{16}	–	–	5	μA
Frequency variation with input voltage at $V_{16-12} > 8$ V	$\frac{\Delta f_o/f_o}{\Delta V_{16-12}}$	–	1	–	%/V
Overcurrent protection input CM (pin 11)					
Input voltage	V_{11-12}	0	–	V_Z	V
Input threshold voltage for single pulse inhibit (current limit mode); $T_{amb} = 25$ °C	V_{T1}	400	–	500	mV
Ratio of threshold voltages for shot down/ slow start and for single pulse inhibit	V_{T2}/V_{T1}	–	1,25	–	
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{11-12} = 250$ mV	$-I_{11}$	–	–	10	μA
Turn-off delay, $I_{15} = 40$ mA; $V_{11-12} = 1{,}2 \times V_{T1}$	t_d	–	–	1,0	μs
Core saturation and overvoltage protection input SAT (pin 13)					
Input voltage	V_{13-12}	0	–	V_Z	V
Input threshold voltage at $T_{amb} = 25$ °C	V_{13-12}	470	600	720	mV
Threshold variation with temperature	$\Delta V/\Delta T$	–	125	–	μV/K
Input current at $V_{13-12} = 250$ mV	$-I_{13}$	–	–	7	μA
ENABLE input EN (pin 10)					
Input voltage					
ON	V_{IN}	2	–	V_Z	V
OFF: TDA1060; TDA1060A; TDA1060T	V_{IL}	0	–	0,8	V
TDA1060B	V_{IL}	0	–	0,6	V
Input current at $V_{10-12} = 0$ V	$-I_{IL}$	20	–	120	μA
Outputs QC and QE (pins 14 and 15)					
Output current	$-I_{14}; I_{15}$	40	–	–	mA
Emitter output voltage	V_{14-12}	–	–	5	V
Collector output voltage at $V_{14-12} = 0$ V; $I_{15} = 40$ mA	V_{15-14}	–	–	500	mV

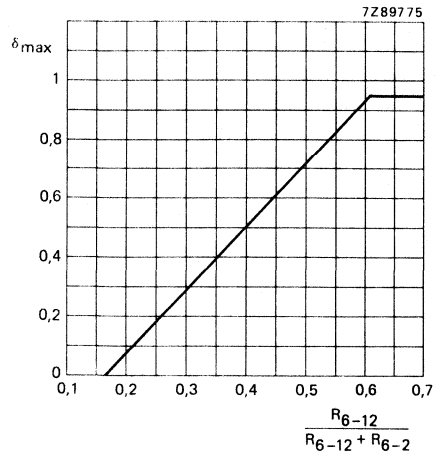


Fig. 4 Maximum duty factor δ_{max} as a function of the voltage divider ratio at the duty factor input DFM.

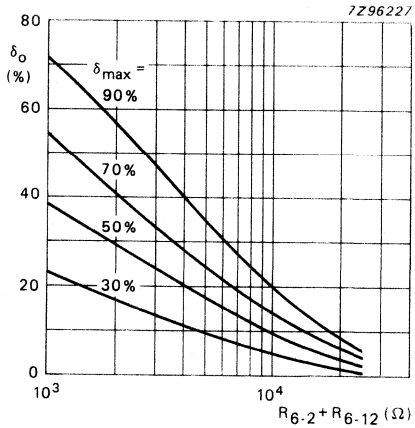


Fig. 5 Soft-start minimum duty factor (δ_o) as a function of R_{6-2} and R_{6-12}.

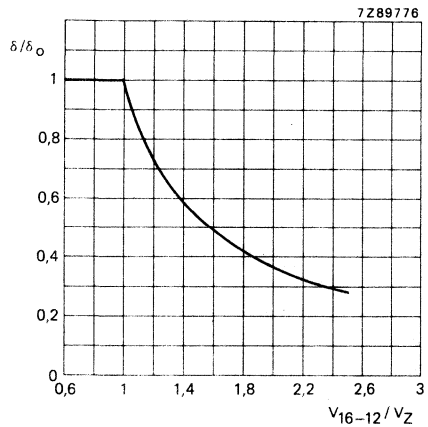


Fig. 6 Feed-forward regulation characteristic. Duty factor δ as a function of the voltage V_{16-12} on the feed-forward input FW. δ_o is the duty factor for $V_{16-12} \leqslant V_Z$.

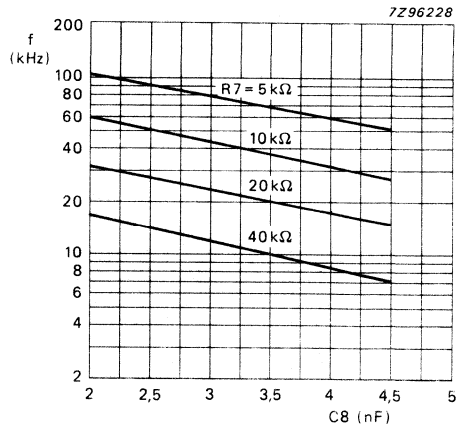


Fig. 7 Typical frequency as a function of C8 (R7 as parameter).

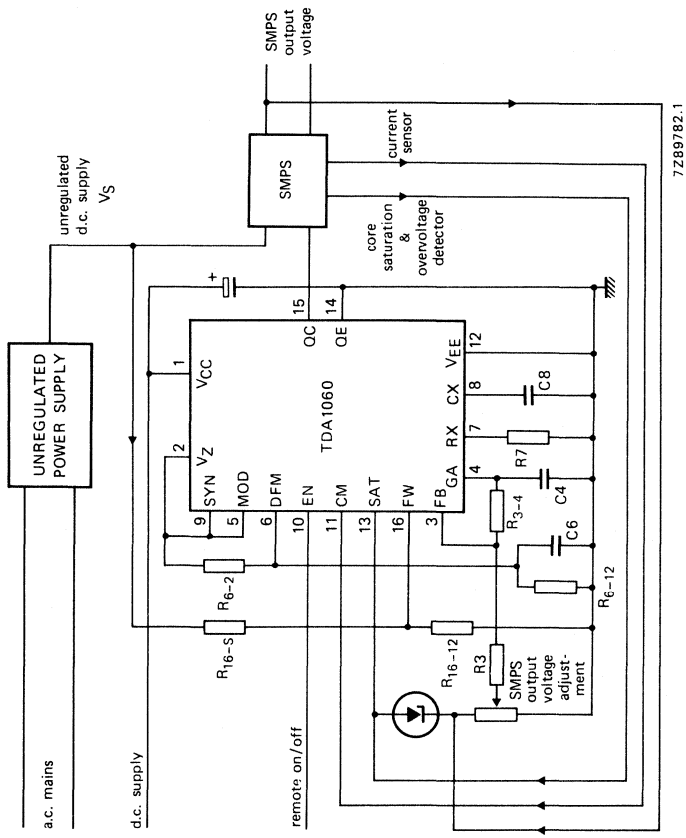


Fig. 8 Connections to the TDA1060 in a switched-mode power supply.

APPLICATION INFORMATION

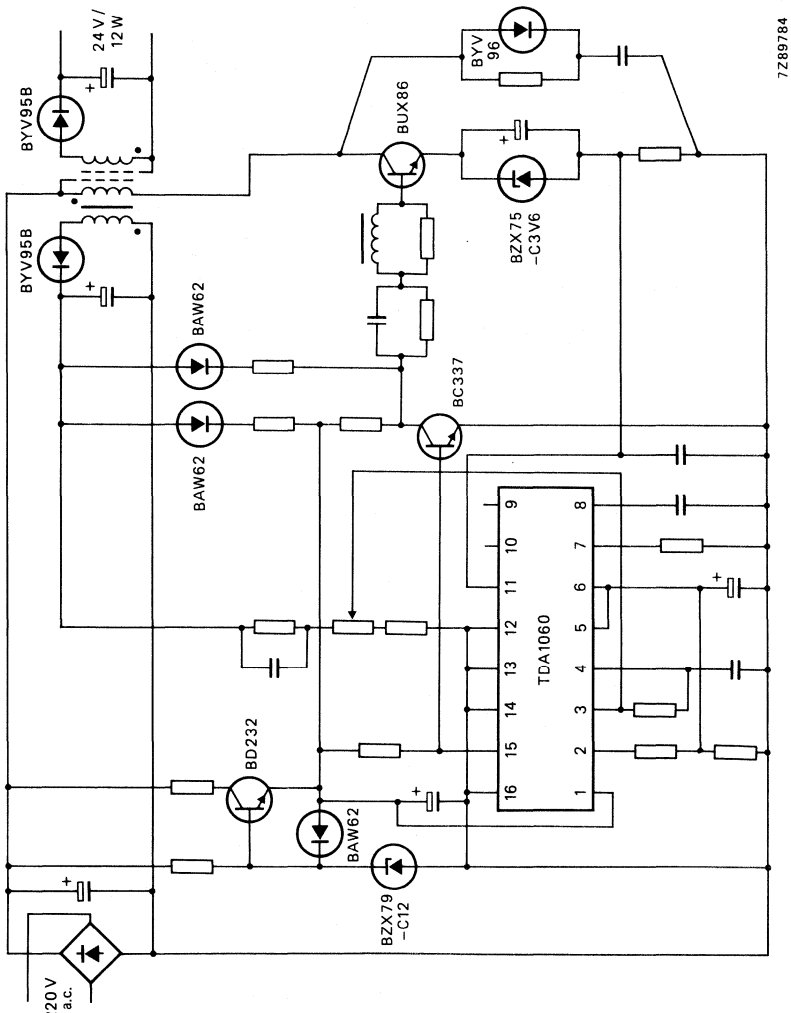


Fig. 9 Application of the TDA1060 in a 24 V, 12 W SMPS with flyback converter.

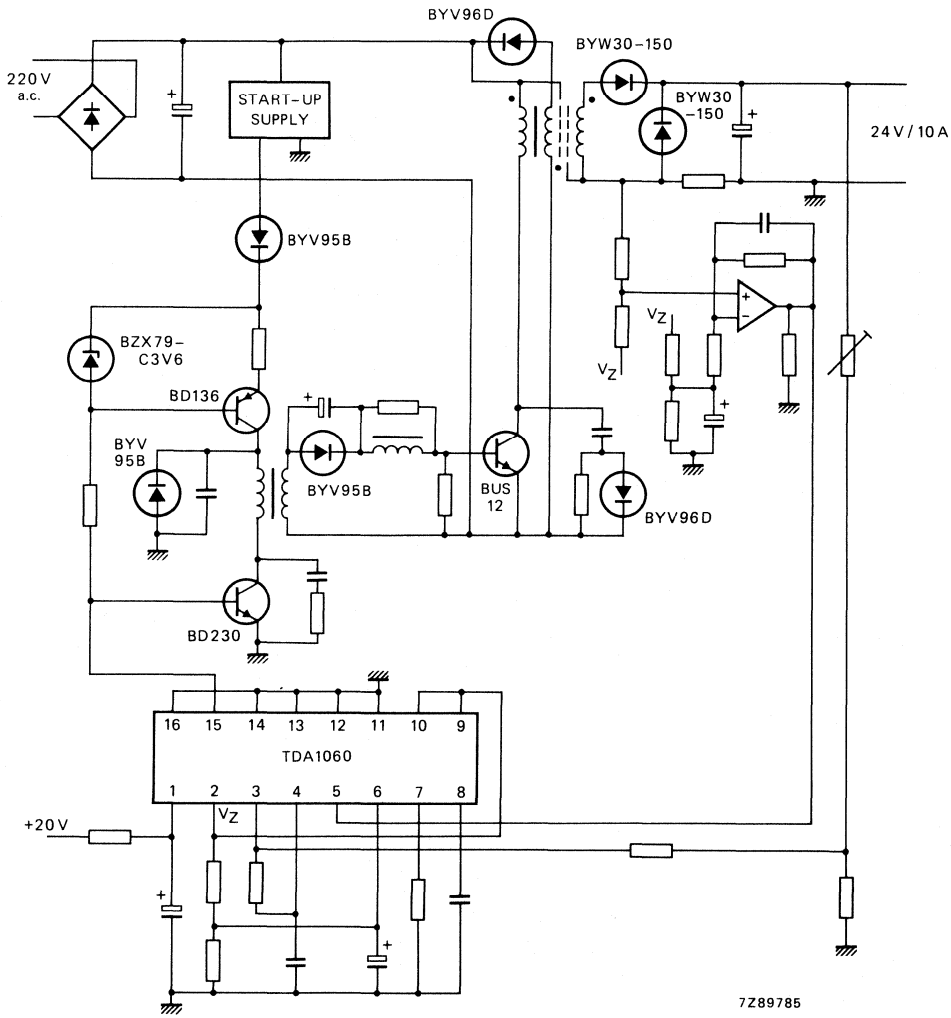


Fig. 10 Application of the TDA1060 in a 24 V, 240 W SMPS with forward converter.

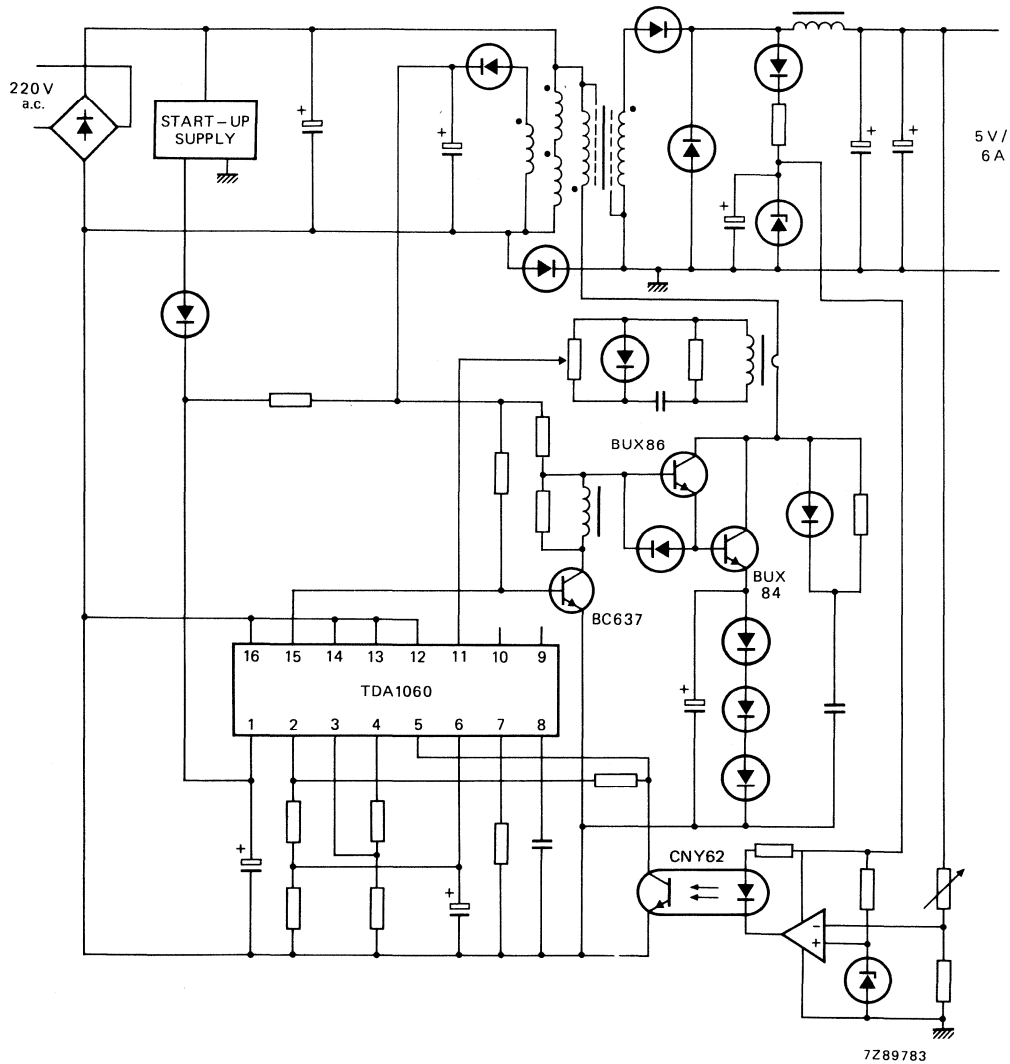


Fig. 11 Application of the TDA1060 in a 5 V, 30 W SMPS with forward converter and with an optocoupler CNY62 for voltage separation.

APPLICATION INFORMATION SUPPLIED UPON REQUEST.

I.F. LIMITING AMPLIFIER, FM DETECTOR AND AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDB1080 is a bipolar integrated circuit comprising a limiting amplifier, a balanced FM detector and a class-B audio amplifier. It is intended for frequencies up to 500 kHz with either narrow-band or wide-band FM. The circuit is especially suited for use in portophone sets, where a low supply voltage, a low supply current and a high sensitivity are of paramount importance.

QUICK REFERENCE DATA

Supply voltage range				
I.F. part	V_{CC1}		2,3 to 3,5	V
A.F. part	V_{CC2}		2,3 to 10	V
Supply current at $V_{CC1} = V_{CC2} = 2{,}5$ V, no signal	$I_{CC1} + I_{CC2}$	typ.	3	mA
Input voltage at onset of limiting	$V_{I1lim(rms)}$	typ.	30	μV
AM rejection at $V_i = 1$ mV	k_{AMR}	typ.	50	dB
Open-loop voltage amplification of audio amplifier	A_{vd}	typ.	200	
Output power of audio amplifier at $V_{CC2} = 9$ V	P_o	typ.	65	mW
Operating ambient temperature range	T_{amb}		−20 to + 70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

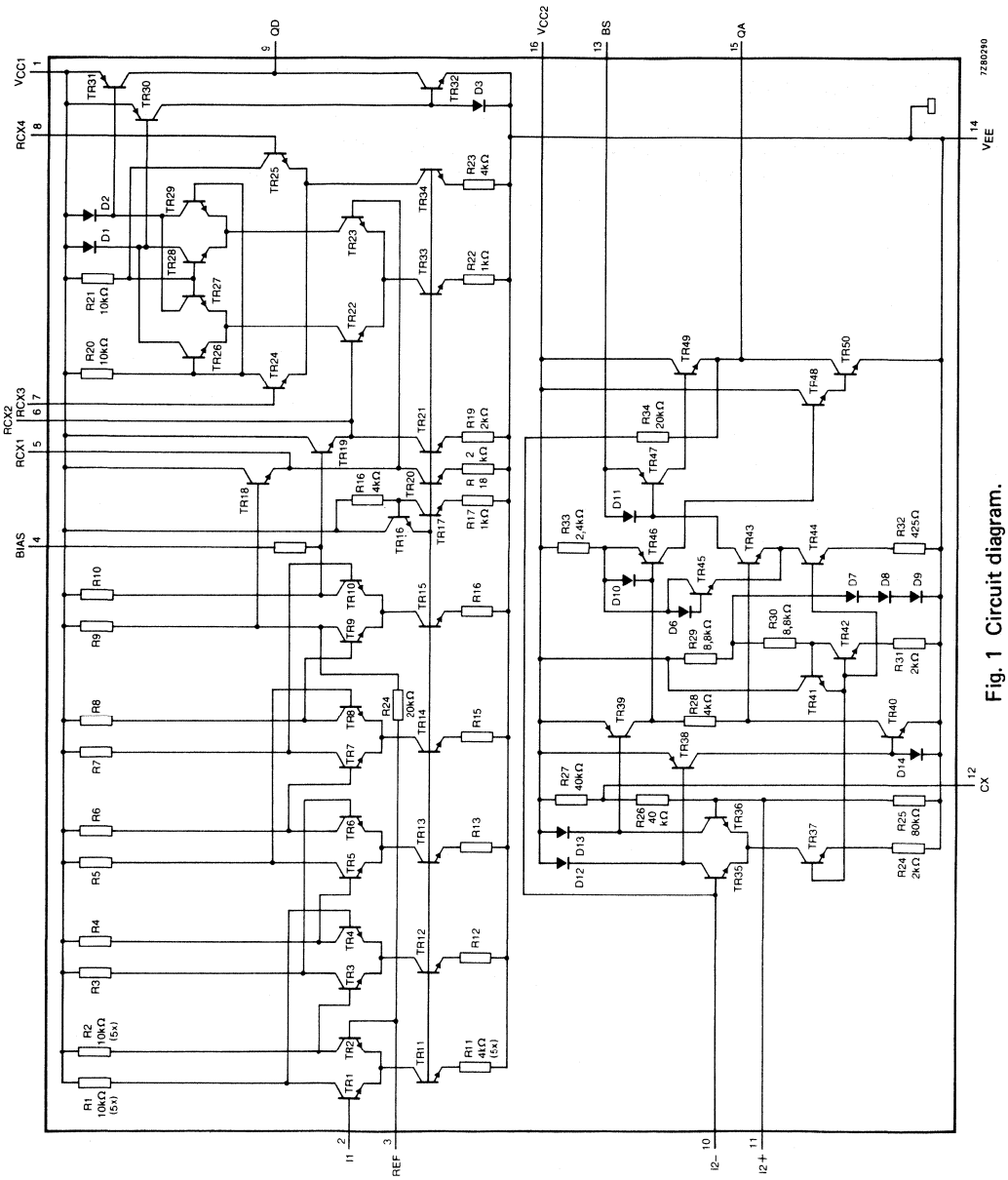


Fig. 1 Circuit diagram.

PINNING

1	V_{CC1}	positive supply, limiting amplifier
2	I1	limiting amplifier input
3	REF	reference input, limiting amplifier
4	BIAS	input biasing output
5	RCX1	external RC network
6	RCX2	external RC network
7	RCX3	external RC network
8	RCX4	external RC network
9	QD	FM detector output
10	I2–	out-of-phase input, audio amplifier
11	I2+	in-phase input, audio amplifier
12	CX	external capacitor
13	BS	bootstrap
14	V_{EE}	ground
15	QA	audio amplifier output
16	V_{CC2}	positive supply, audio amplifier

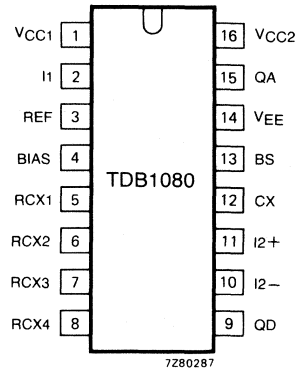


Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The TDB1080 consists of two parts that may be used independently, viz. a limiting i.f. amplifier with balanced FM detector, and a class-B audio amplifier.

Supply

The two parts of the circuit have a common-ground pin V_{EE} but separate supply pins V_{CC1} and V_{CC2}. The limiting amplifier and detector may be used with a supply voltage up to 3,5 V, the audio amplifier up to 10 V. The circuit is built to a large extent on the basis of long-tailed pairs with current sources in their tails. Thanks to the stabilizer diodes (D7, D8 and D9) the supply current of the audio amplifier varies little with the supply voltage. This permits the circuit to be used over a wide supply voltage range without an excessive battery drain as a result.

Limiting amplifier inputs I1 and REF and biasing output BIAS (pins 2, 3 and 4)

The limiting amplifier has differential inputs I1 and REF. I1 is intended to be used as an input; it should be biased externally by connecting it to the input biasing output BIAS via a resistor or an inductor. The reference input REF is biased internally; it should be decoupled by connecting a capacitor from REF to ground.

The onset of limiting is specified as the input voltage giving 3 dB gain reduction.

External RC network pins RCX1 to RCX4 (pins 4 to 8)

The TDB1080 contains a quadrature detector which requires an RC phase shifting network. This has to be connected to RCX1, RCX2, RCX3 and RCX4 as shown in Fig. 4. The component values have to be chosen in accordance with the i.f. centre frequency.

Audio amplifier inputs I2+ and I2– (pins 11 and 10)

The audio amplifier has differential inputs I2+ and I2– which are biased internally.

FUNCTIONAL DESCRIPTION (continued)

External capacitor pin CX (pin 12)

The internal biasing network for input I2+ should be decoupled by connecting an external capacitor between CX and ground.

Audio amplifier output QA and bootstrap pin BS (pins 15 and 13)

The audio amplifier has a class-B output stage. The maximum output voltage swing is obtained by connecting a capacitor between the bootstrap pin BS and the output QA and the load from BS to V_{CC2} (see Fig. 4).

The maximum output power varies from typ. 15 mW at V_{CC2} = 2,5 V to typ. 65 mW at V_{CC2} = 9 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages, d.c.	V_{CC1}	max.	5 V
	V_{CC2}	max.	10 V
Supply current	$I_{CC1} + I_{CC2}$	max.	50 mA
Total power dissipation	P_{tot}	see Fig. 3	
Storage temperature range	T_{stg}	−55 to + 125	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C

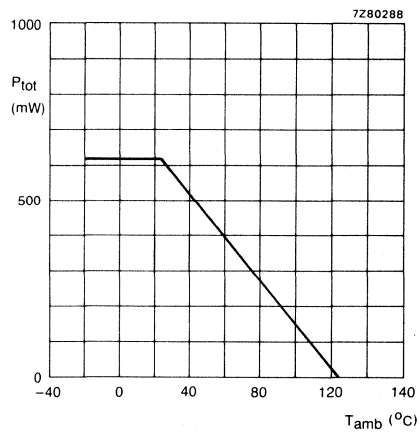


Fig. 3 Power derating curve.

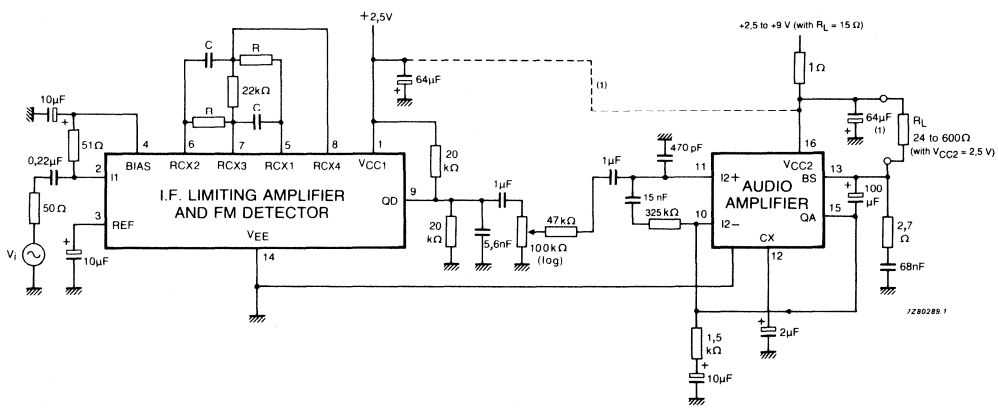
CHARACTERISTICS

$V_{CC1} = V_{CC2} = 2,5$ V; $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz; $f_m = 1$ kHz; $T_{amb} = 25\ ^oC$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies V_{CC1} and V_{CC2} (pins 1 and 16)					
Supply voltages	V_{CC1}	2,3	2,5	3,5	V
	V_{CC2}	2,3	2,5	10	V
Supply currents					
at $V_{CC1} = 2,5$ V	I_{CC1}	–	1,5	2	mA
at $V_{CC2} = 2,5$ V, no signal	I_{CC2}	–	1,5	2	mA
at $V_{CC2} = 9$ V, no signal	I_{CC2}	–	3,5	–	mA
Limiting amplifier input I1 (pin 2)					
Input impedance	$\lvert z_{id} \rvert$	15	–	–	kΩ
Input voltage for onset of limiting (3 dB gain reduction)	$V_{I1lim(rms)}$	–	30	–	μV
Source impedance (between I1 and REF)	$\lvert Z_S \rvert$	–	–	5	kΩ
A.M. suppression					
at $\Delta f_i = 70$ Hz; $f_m = 1$ kHz; m = 0,3; $R_S = 50\ \Omega$					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	50	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
$R_S = 5$ kΩ					
at $V_{I1(rms)} = 300\ \mu$V	k_{AMR}	–	30	–	dB
at $V_{I1(rms)} = 1$ mV	k_{AMR}	–	40	–	dB
at $V_{I1(rms)} = 10$ mV	k_{AMR}	–	50	–	dB
FM Detector output QD (pin 9)					
Output voltage at $d_{tot} = 0,5\%$;					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	$V_{QD(rms)}$	100	–	–	mV
Signal-to-noise ratio					
at $f_i = 95$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB
at $f_i = 250$ kHz; $\Delta f = \pm 50$ kHz	S/N	70	–	–	dB

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Audio amplifier					
Open-loop voltage amplification	A_{vd}	–	200	–	
variation with frequency, f = 50 Hz to 15 kHz	ΔA_{vd}	−1,5	–	+ 1,5	dB
Load resistance	R_L	24	–	600	Ω
Output voltage at R_L = 24 Ω; d_{tot} = 1%	$V_{QA(rms)}$	–	600	–	mV
Total distortion at R_L = 24 Ω; $V_{QA(rms)}$ = 500 mV	d_{tot}	–	0,5	1	%
Output power at V_{CC2} = 9 V; R_L = 115 Ω; d_{tot} = 5%	P_{QA}	–	65	–	mW
Signal-to-noise ratio at R_L = 115 Ω; V_o = 600 mV; f = 0,5 to 11 kHz; 80 dB/octave cut-off filter	S/N	70	–	–	dB



(1) If V_{CC2} is equal to V_{CC1} pin 16 can be connected to pin 1 and the capacitor to pin 16 can be omitted.

Fig. 4 Test circuit and typical application of the TDB1080. For f_i = 95 kHz R = 100 kΩ and C = 82 pF, for f_i = 250 kHz R = 33 kΩ and C = 47 pF.

13-BIT SERIES-PARALLEL CONVERTER

GENERAL DESCRIPTION

The TEA1017 is a bipolar integrated circuit intended to drive displays, triacs and relays and small stepper motors. The data is serially shifted into the device and is stored in 13 latches that drive the outputs.

Features

- TTL and CMOS compatible inputs
- Outputs drive load in both directions
- Power-on reset makes outputs floating
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,5 to 18	V
Output current, each output	I_{OL}; $-I_{OH}$	max.	80	mA
Clock frequency	f_{CLK}	max.	50	kHz
Operating ambient temperature range	T_{amb}		0 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102H).

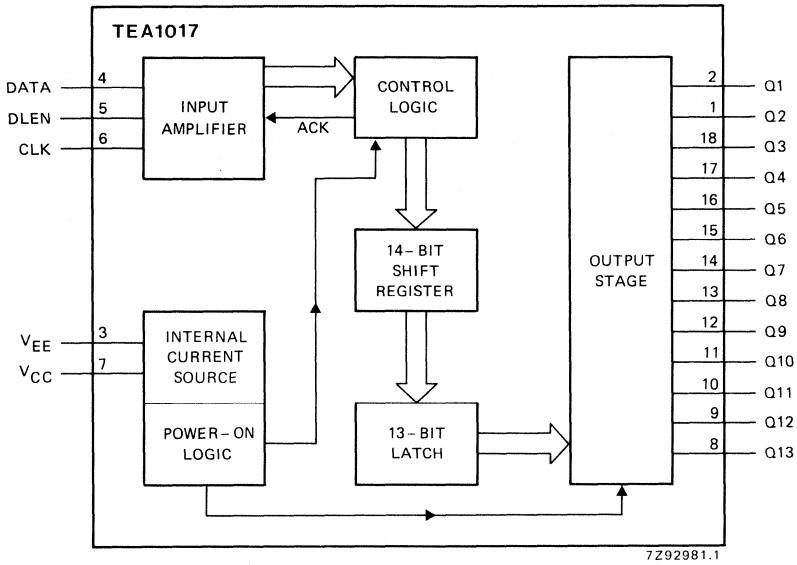


Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The control logic performs a key function in this device. It checks whether the input information has the correct format: a DLEN signal that has been HIGH during 14 clock pulses, and a DATA signal with its first bit LOW.
When the format is found to be correct, the 15th clock pulse makes the control logic generate a signal that loads the content of the first 13 bits of the shift register into 13 latches. These drive the output stages.

"Acknowledge" (pin 4)

After the 15th clock pulse an acknowledge signal drives the DATA pin to LOW. To use this information the DATA should be programmed HIGH and an open collector-device, or a series resistor should be used on the DATA-input. This signal is valid till the next clock pulse, LOW-to-HIGH transition, see Fig. 3.

Supply V_{CC} (pin 7)

The supply current of the TEA1017 is regulated internally. This permits the circuit to be used over a very wide range of supply voltages, viz. 4,5 to 18 V, with little variation of supply current.

The circuit has a power-on reset arrangement that resets the circuit and sets the outputs to a high-impedance state. It requires a rise-time of the supply larger than 3 us/V.

DATA input (pin 4)

The circuit requires input information on the DATA input consisting of 14 bits, the first bit being LOW. This information should be synchronous with the clock pulse.
Data is loaded into the shift register at HIGH-to-LOW transitions of the clock pulse.

Data line enable input DLEN (pin 5)

A HIGH level on the DLEN input enables the shift register. This HIGH level should have a duration of 14 clock pulses (see Fig. 3).
After the DLEN input has returned to LOW the subsequent (15th) clock pulse transfers the contents of the shift register to the latches and then to the outputs.

Clock input CLK (pin 6)

The shift register shifts at the HIGH-to-LOW transitions of the clock pulse. The clock signal may be a continuously running clock or a clock burst of 15 clock pulses.

Outputs Q1 to Q13

The outputs are capable of supplying a load current in both directions, i.e. they can drive a load to the supply (V_{CC}) or to ground (V_{EE}).

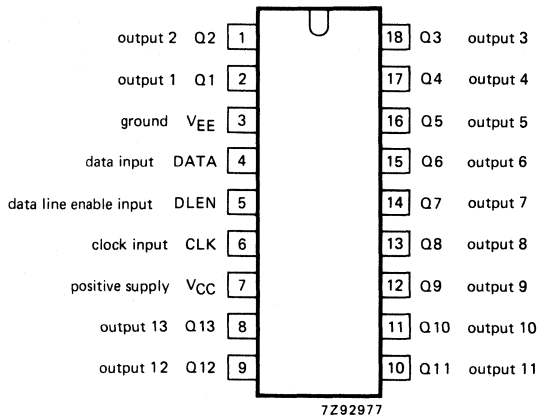


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	18	V
Input voltage range, all inputs	V_I	$-0,3$ to V_{CC}	$+0,3$	V
Output current, all outputs				
HIGH	$-I_{OH}$	max.	150	mA
LOW	I_{OL}	max.	150	mA
Total power dissipation *	P_{tot}	max.	1,4	W
Storage temperature range	T_{stg}	-40 to	$+150$	°C
Operating ambient temperature range	T_{amb}	0 to +	80	°C

* See Fig. 4.

CHARACTERISTICS

V_{CC} = 4,5 to 18 V; V_{EE} = 0 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply current					
during normal operation, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	45	60	mA
at V_{CC} = 18 V	I_{CC}	–	50	70	mA
during power-on blanking, unloaded					
at V_{CC} = 4,5 V	I_{CC}	–	1,5	2	mA
at V_{CC} = 18 V	I_{CC}	–	5	7	mA
Supply voltage rise time to ensure power on reset		3	–	–	μs/V
Clock input CLK (pin 6)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{CLKH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{CLKL} = 0,4 V	$-I_{IL}$	–	–	10	μA
Clock pulse duration					
HIGH	t_{WH}	8	–	–	μs
LOW	t_{WL}	10	–	–	μs
DATA input (pin 4)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{IH} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{IL} = 0,4 V	$-I_{IL}$	–	–	10	μA
DATA input in sink current					
ACK = TRUE	I_{DACK}	1	–	–	mA
Data line enable input DLEN (pin 5)					
Input voltage					
HIGH	V_{IH}	2	–	–	V
LOW	V_{IL}	–	–	0,8	V
Input current					
HIGH at V_{5-3} = 2 V	I_{IH}	–	–	10	μA
LOW at V_{5-3} = 0,4 V	$-I_{IL}$	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Outputs Q1 to Q13					
Output voltage during normal operation					
HIGH at $-I_{OH}$ = 80 mA	V_{OH}	$V_{CC}-1,5$	–	–	V
LOW at I_{OL} = 80 mA	V_{OL}	–	–	1	V
Output current during power-on reset					
HIGH	$-I_{OH}$	–	–	10	μA
LOW	I_{OL}	–	–	10	μA
Rise and fall times: no maximum					
Minimum times as V_{CC} = 4,5 volts (see Fig. 3)					
Set-up time ENABLE	t_{SUDL}	2,8	–	–	μs
Hold time ENABLE	t_{HDL}	5,0	–	–	μs
Set-up time DATA	t_{SDA}	0	–	–	μs
Hold time DATA	t_{HDA}	2,8	–	–	μs
Set-up time LOAD	t_{SLO}	1,4	–	–	μs
Pulse width LOW	t_{WL}	10	–	–	μs
Pulse width HIGH	t_{WH}	8	–	–	μs
Max. clock input frequency = $1/(t_{WH} + t_{WL})$	f_{max}	–	–	50	kHz
Propagation delay					
clock to outputs	t_{PCQ}	–	–	8,5	μs
acknowledge	t_{PCA}	–	–	6	μs
acknowledge release	t_{PCAR}	–	–	6	μs

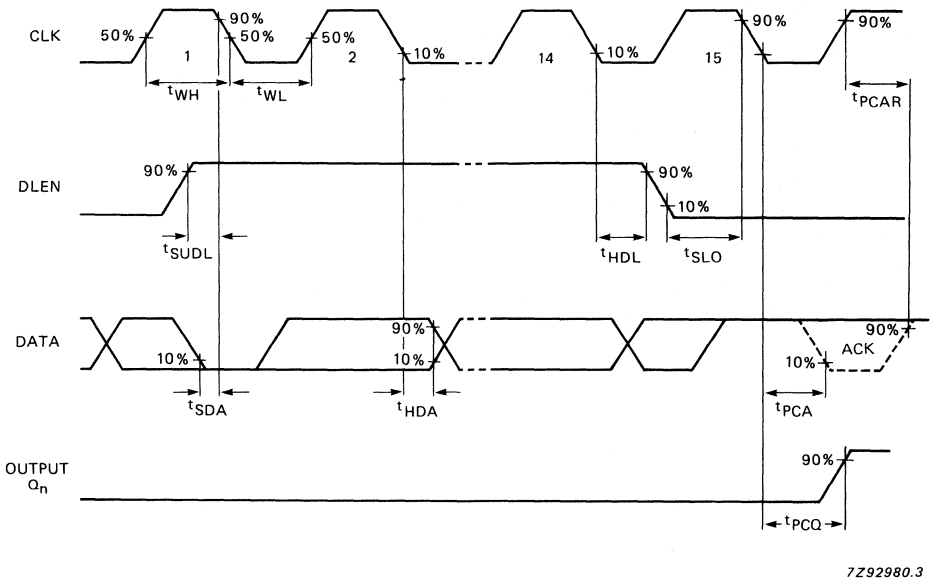


Fig. 3 Bus timing characteristics.

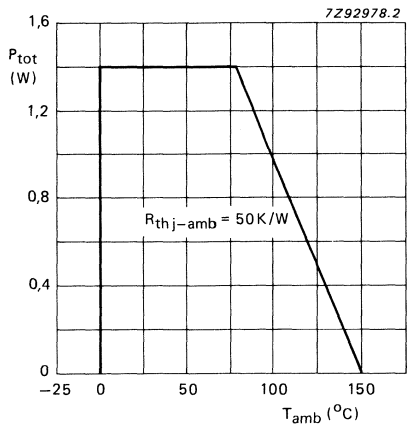


Fig. 4 Derating curve.

APPLICATION INFORMATION

1. From the buffer-capacitors C1 of the power supply the supply connections to the TEA1017 and the loads should be separated. An extra capacitor of 10 μF with good high-frequency characteristics should be mounted across the V_{CC} and V_{EE} connections as close as possible to the TEA1017.
2. If no use is made of the acknowledge information it is advised to program the data-output from the controller to LOW during the time ACK is valid. To use the acknowledge information the data-output has to be programmed HIGH. When a push-pull controller device is used a series resistor has to be connected in the data-line between the controller and TEA1017.
   The ACK may be sensed on the TEA1017-side of this resistor. See Fig. 5.

Note. ACK is removed from the data-line after the next LOW-to-HIGH transition of the clock-line with a maximum delay of 6 μs. (t_{PCA} maximum).

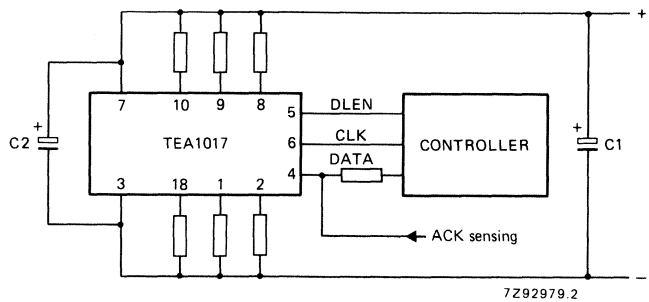


Fig. 5 TEA1017 with 3 loads to V_{CC} Q = 0 and 3 loads to V_{EE} Q = 1.

CONTROL CIRCUIT FOR SMPS

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

Features

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14 V
Supply current	I_{CC}	max.	13 mA
Output pulse repetition frequency range	f_o	1 Hz to 100	kHz
Output current LOW	I_{OL}	max.	1 A
Operating ambient temperature range	T_{amb}	−25 to +125	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

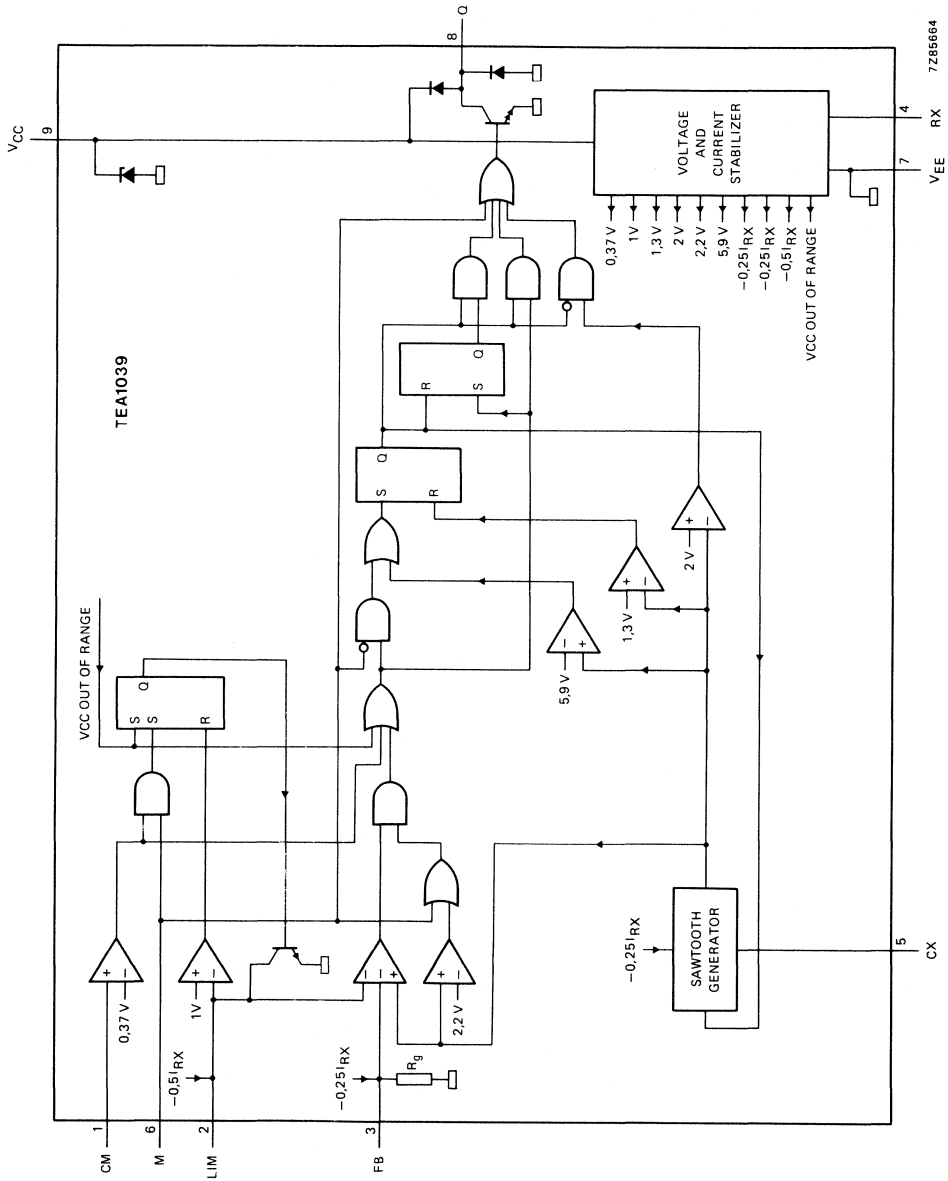


Fig. 1 Block diagram.

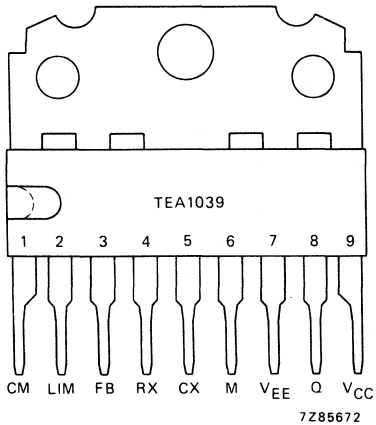


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to +20 V
Supply current range, current source	I_{CC}	−30 to +30 mA
Input voltage range, all inputs	V_I	−0,3 to +6 V
Input current range, all inputs	I_I	−5 to +5 mA
Output voltage range	V_{8-7}	−0,3 to +20 V
Output current range		
output transistor ON	I_8	0 to 1 A
output transistor OFF	I_8	−100 to + 50 mA
Storage temperature range	T_{stg}	−55 to +150 °C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to +125 °C
Power dissipation (see Fig. 3)	P_{tot}	max. 2 W

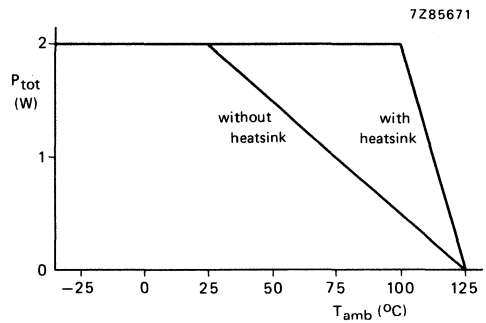


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	–0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	–5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

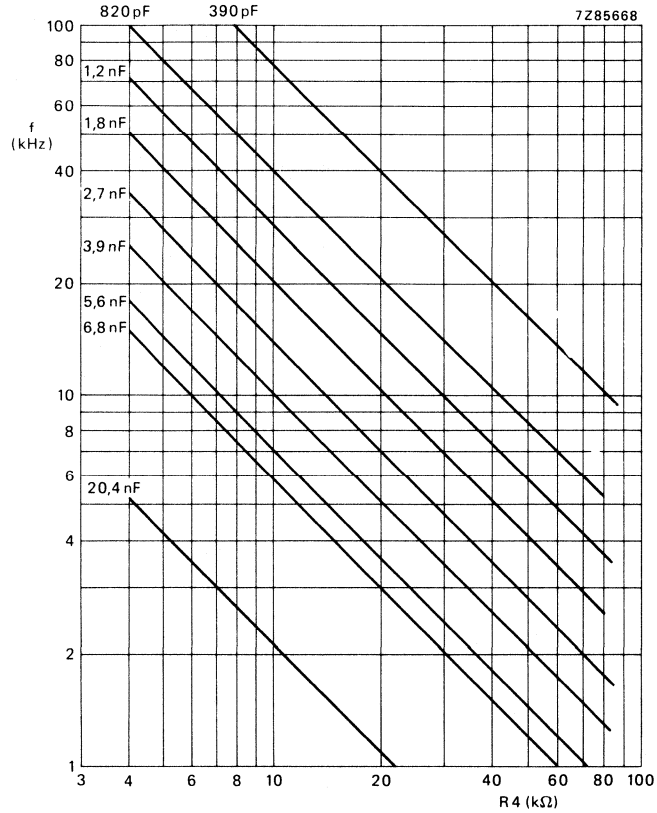


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

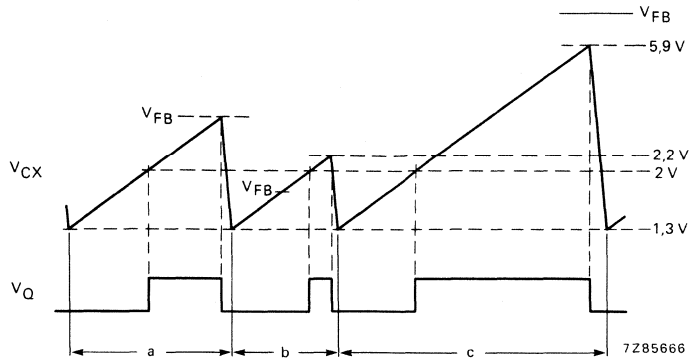


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

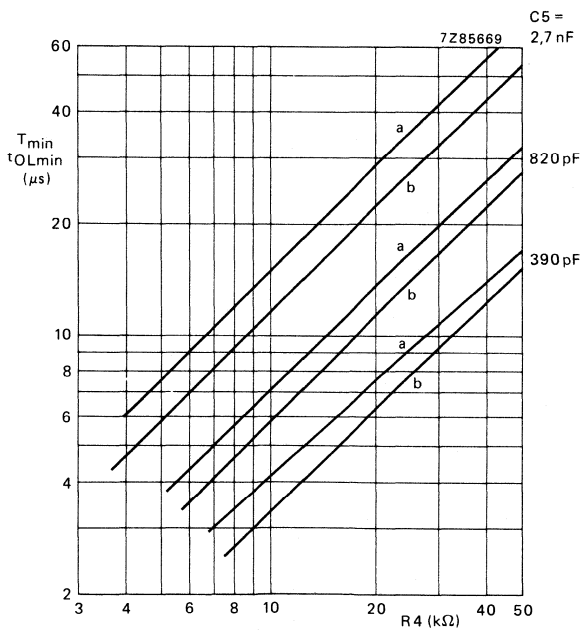


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

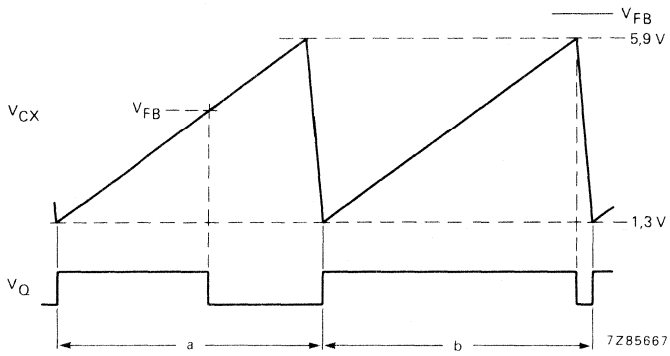


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

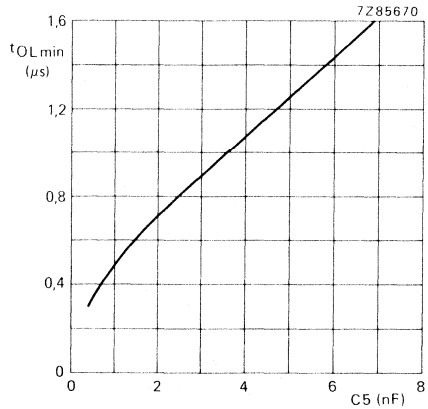


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

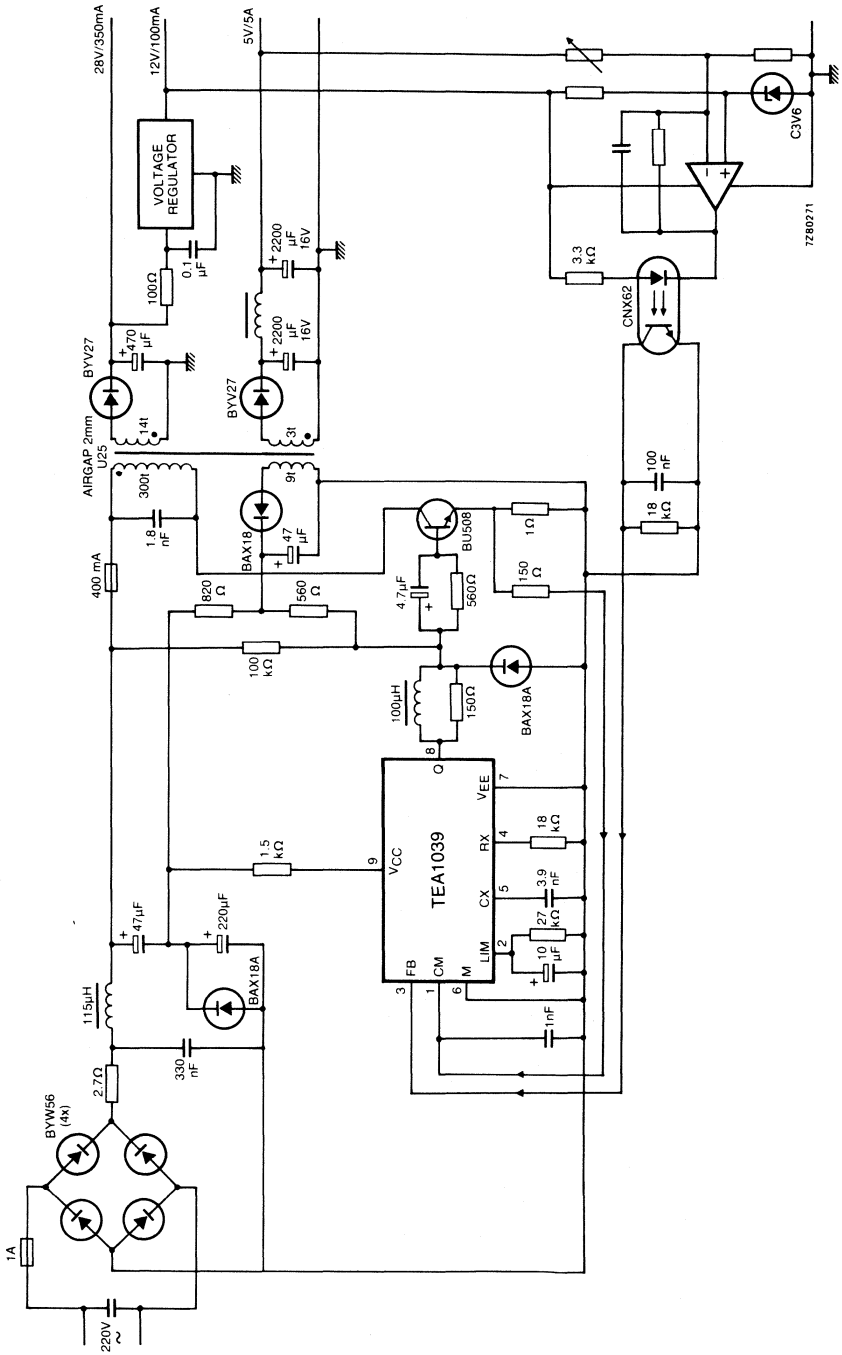


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

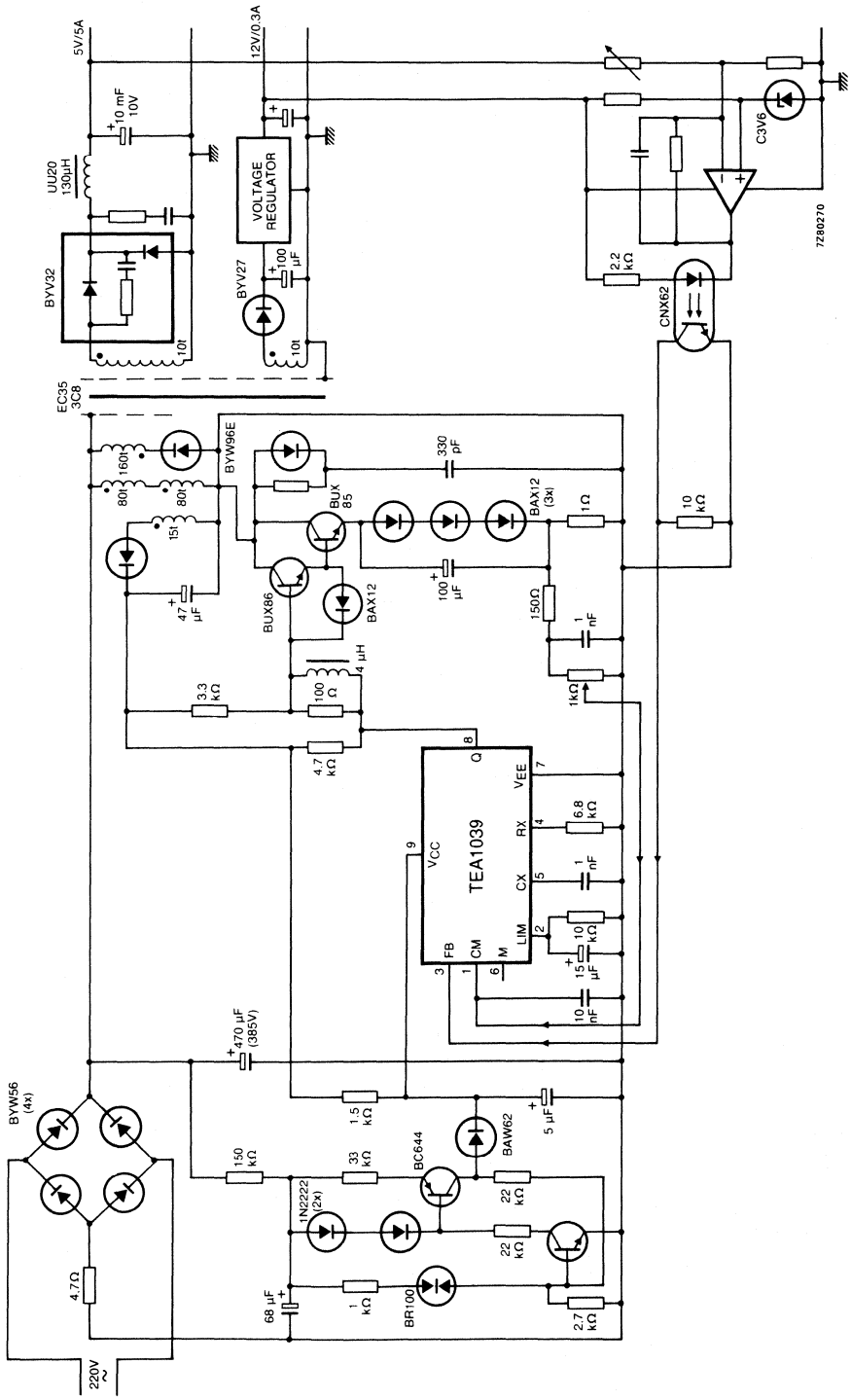


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

CODED LOCKING CIRCUIT FOR SECURITY SYSTEMS

GENERAL DESCRIPTION

The TEA5500 is a coder/decoder circuit, for security systems. The system has the ability to transmit a complex code between a coding and decoding unit by infrared radiation. The device can operate as a coder or decoder depending on the external circuitry connected to the data input. The code is made by the 10 input pins E1 to E10 by connecting them either to ground (LOW) or to the positive supply (HIGH), or leaving them floating (∞). This allows $3^{10}-2$ combinations. Two combinations are prohibited; E1 to E10 = HIGH and E1 to E9 = HIGH, E10 = LOW.

Coding

In coding mode the data input is connected to V_P and both outputs (S1, S2) are connected to a pnp output transistor which drives an infrared radiation emitting diode.
After every start the coder completes three coding runs then stops automatically.

Decoding

In decoding mode an infrared sensitive diode is connected to the data input via an amplifier. If the input data is recognized, one of the outputs is activated for a predetermined time after which the following start will activate the other output.
If the input data is not recognized, neither of the outputs are activated and after the third coding run is completed the data input of the decoder is temporarily closed.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 16)	V_P = 4.5 V	V_P	3.0	4.5	6.5	V
Supply current (pin 16)		I_P	1.8	2.5	3.2	mA
Operating ambient temperature range		T_{amb}	−40	−	+ 80	°C
Storage temperature range		T_{stg}	−50	−	+ 150	°C
Total power dissipation		P_{tot}	−	−	500	mW

PACKAGE OUTLINE

16-lead DIL; plastic SOT-38).

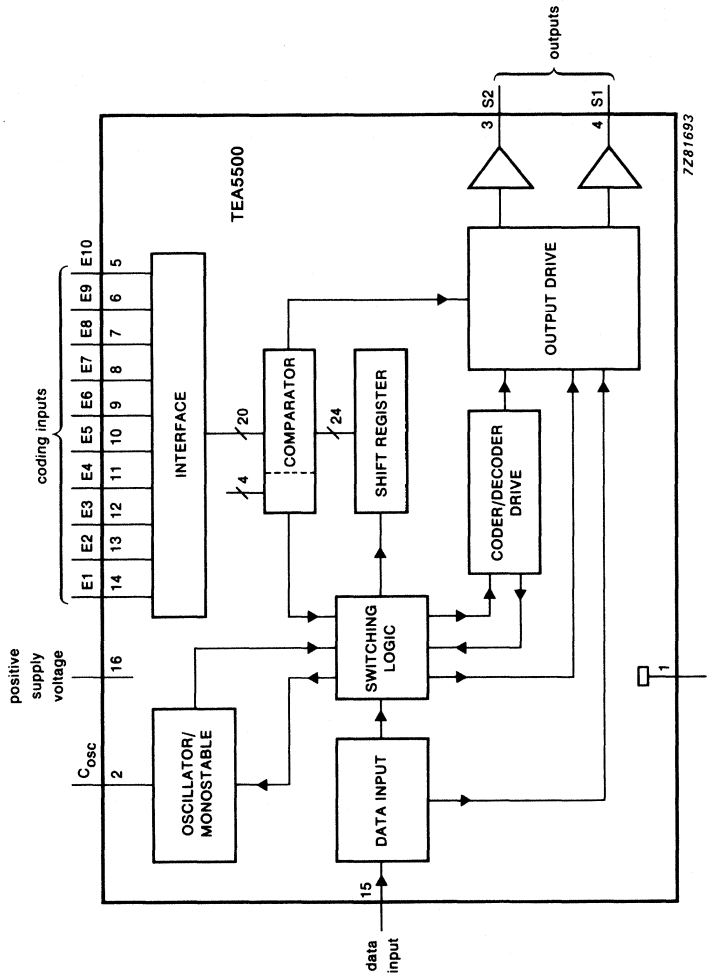


Fig. 1 Block diagram.

PINNING

Pin functions

pin	mnemonic	description
1	GND	negative supply voltage or ground
2	C_{osc}	oscillator capacitor
3	S2	output 2
4	S1	output 1
5	E10	coding inputs
6	E9	
7	E8	
8	E7	
9	E6	
10	E5	
11	E4	
12	E3	
13	E2	
14	E1	
15	DATA	data input
16	V_P	positive supply voltage

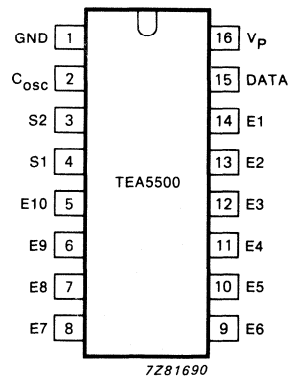


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 16)	V_P	–	7	V
Supply current (pin 16)	I_P	0	50	mA
Input voltage (pins 2 and 5 to 15)	V_I	−0.3	V_P + 0.3	V
Output voltage (pins 3 and 4)	V_O	−0.3	16	V
Total power dissipation	P_{tot}	–	500	mW
Storage temperature range	T_{stg}	−50	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 80	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\,j\text{-}a} = 125$ K/W

CHARACTERISTICS

T_{amb} = 25 °C; voltages with respect to pin 1; unless otherwise specified

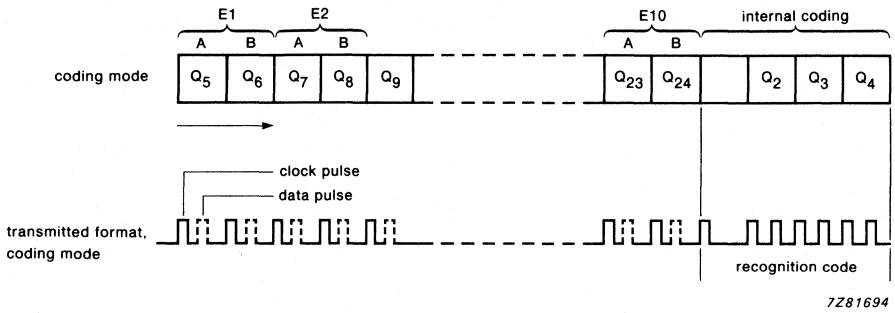
parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 16)		V_P	3	4.5	6.5	V
Supply current	V_P = 4.5 V	I_P	1.8	2.5	3.2	mA
Output current (pins 3 and 4)	V_P = 4.5 V	I_O	25	–	–	mA
Inputs E1 to E10						
Input voltage HIGH		V_{IH}	V_P –0.3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input voltage floating		V_{IFL}	1	–	V_P –1	V
Input current HIGH		I_{IH}	3	4.5	8	μA
Input current LOW		I_{IL}	–4.5	–7.5	–10	μA
Input current floating		I_{IFL}	–	–	2	μA
Data input						
Input voltage						
for decoding mode HIGH		V_{dc}	V_P –0.6	V_P	V_P + 0.3	V
for decoding mode LOW		V_{dd}	–	–	0.5	V
Input current						
in coding mode		I_{dc}	9.5	14	18.5	μA
in decoding mode HIGH	V_P = 4.5 V	I_{ddH}	–	–	2	μA
in decoding mode LOW	V_P = 4.5 V	I_{ddL}	–9.5	–14	–18.5	μA
Minimum pulse width of DATA input signal		τ_{dp}	2	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator characteristics	$V_P = 4.5$ V					
Switching voltage thresholds						
high level		V_{th}	3.10	3.32	3.50	V
low level		V_{tl}	0.65	0.71	0.90	V
Input current						
after switching high level		I_{th}	27	36	45	μA
after switching low level		I_{tl}	−6.7	−9	−11.3	μA
Ratio I_{th}/I_{tl}		ΔI_{osc}	3	4	5	
Duration of oscillator pulse						
in coding mode	note 1	τ_c	10	$0.4 \cdot C_{osc}$(pF)	–	μs
in decoding mode		τ_d	$3 \cdot \tau_c$	$0.4 \cdot C_{osc}$(pF)	$5 \cdot \tau_c$	μs
Oscillator capacitor						
in coding mode	notes 1 and 2	C_{osc}	56	–	–	pF
Influence of temperature on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta T}$	–	0.002	–	$^oC^{-1}$
Influence of supply voltage on duration of oscillator pulse		$\frac{\Delta\tau_c/\tau_c}{\Delta V_P}$	–	–	0.16	V^{-1}
Zener diode voltage across supply		V_z	6	–	8	V

Notes to the oscillator characteristics

1. Minimum value coder – capacitor must provide minimum pulse width of DATA pulse τ_{dp} (= $1/5\,\tau_c$).
2. Ratio coder/decoder capacitor 1:3.

DEVELOPMENT DATA



coding	E1	E2	E3	-----	E8	E9	E10		∞	L	H
decoding	E10	E9	E8	-----	E3	E2	E1		L	∞	H

E	A	B	Q_A	Q_B
L	1	0	0	1
∞	0	1	1	0
H	1	1	0	0

example

coding	E1 = L	E1 = H	E3 = ∞	E7 = H	-----	E9 = L E10 = ∞
decoding	E10 = ∞	E9 = H	E8 = L	E7 = H	-----	E2 = ∞ E1 = L

Fig. 3 Coding diagram.

DEVELOPMENT DATA

TIMING

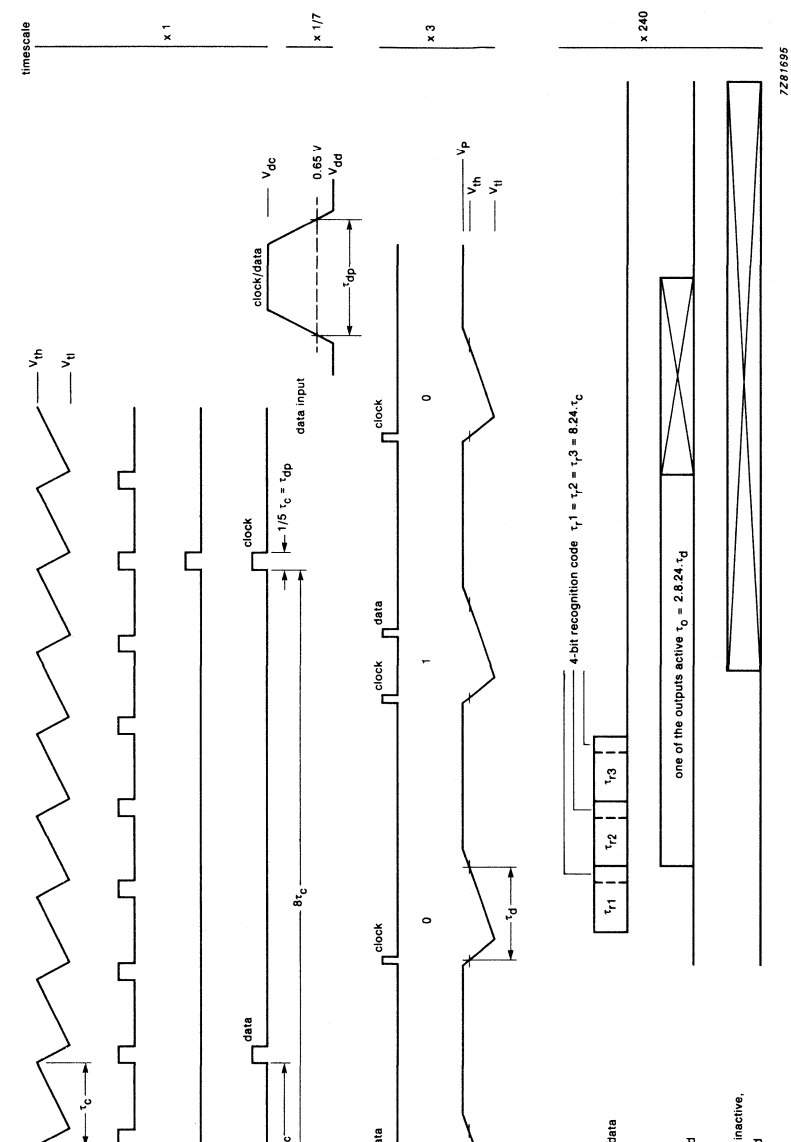


Fig. 4 Timing diagram of TEA5500.

APPLICATION INFORMATION

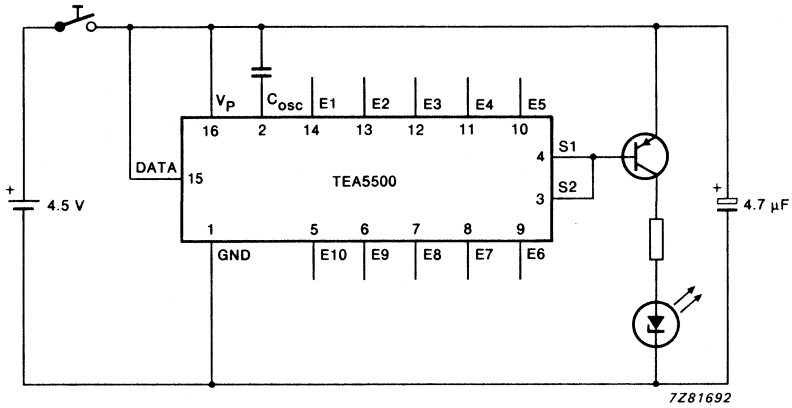


Fig. 5 Application diagram; coding mode.

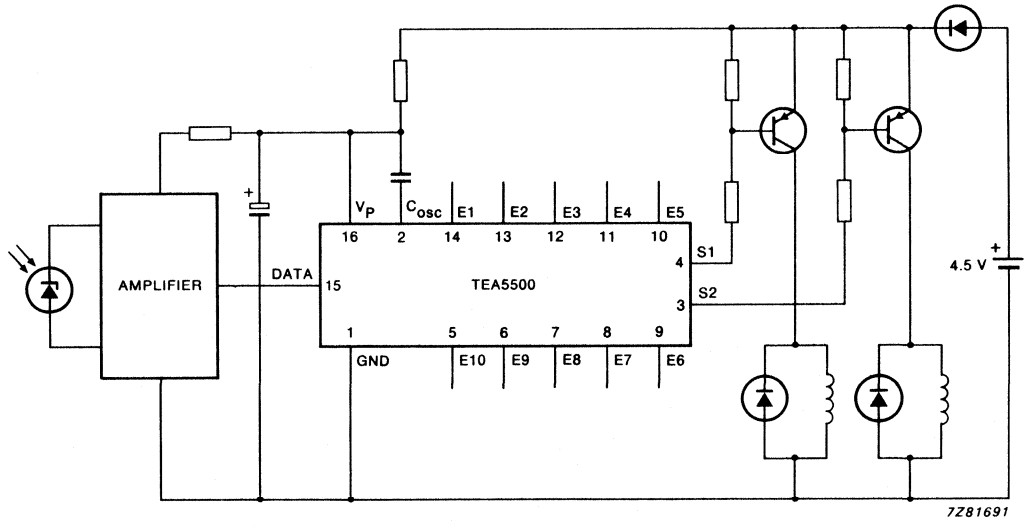
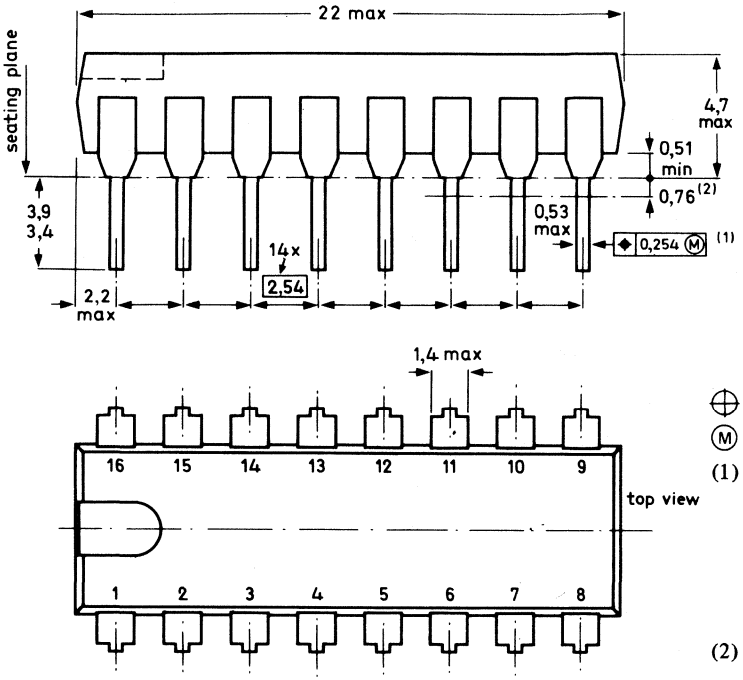


Fig. 6 Application diagram; decoding mode.

PACKAGE INFORMATION

Package outlines
Soldering

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

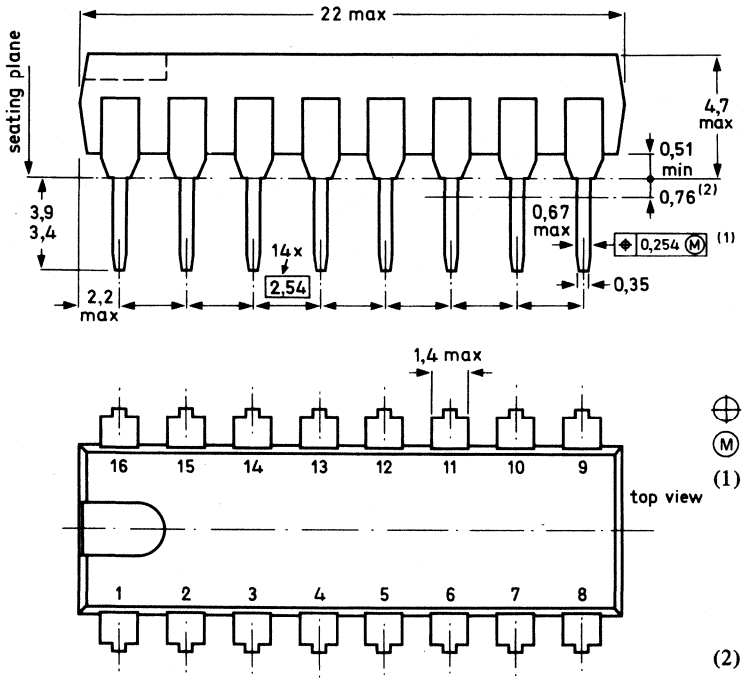
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38A)



Dimensions in mm

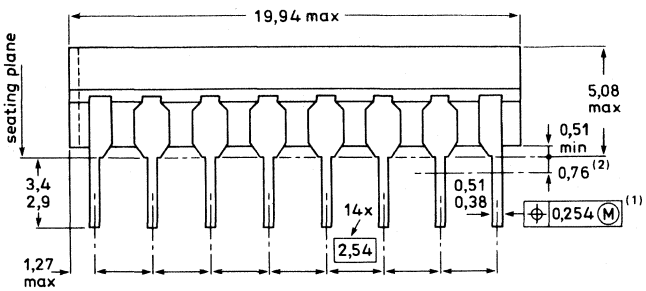
⊕ Positional accuracy.

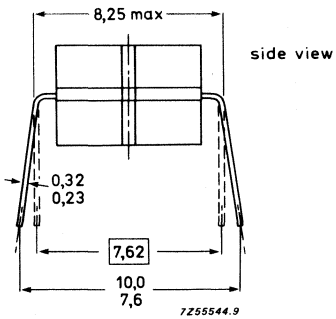
Ⓜ Maximum Material Condition.

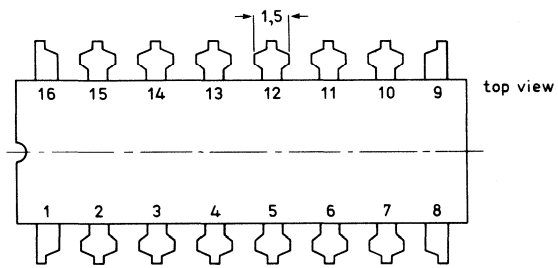
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT74)







Dimensions in mm

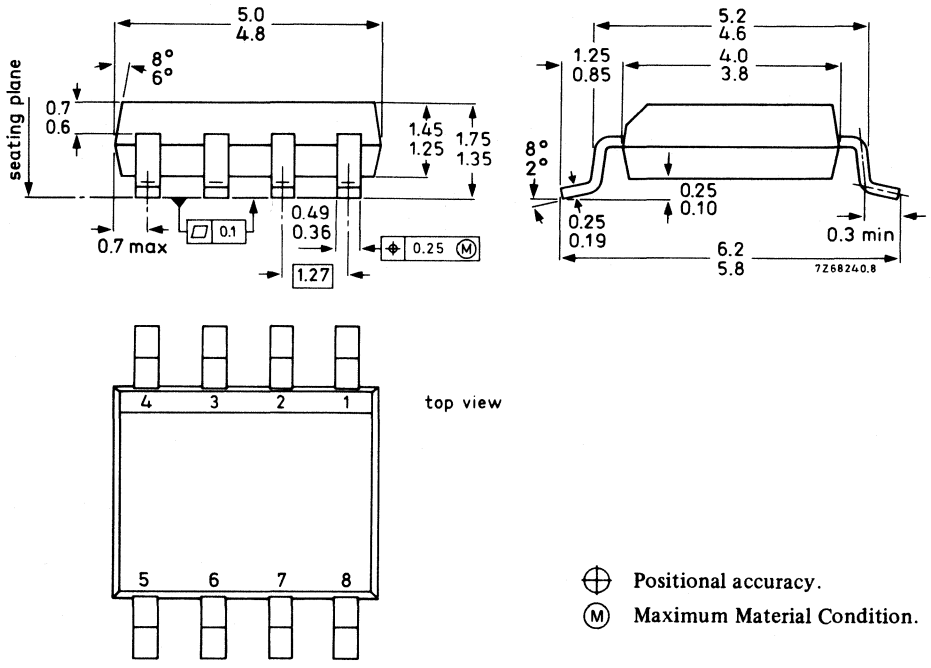
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

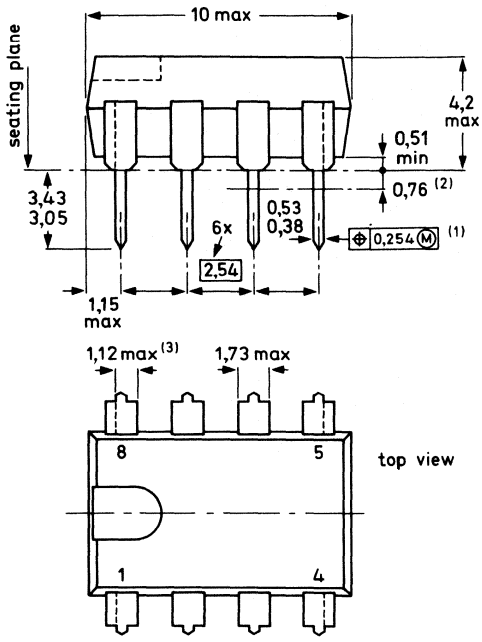
(2) Lead spacing tolerances apply from seating plane to the line indicated.

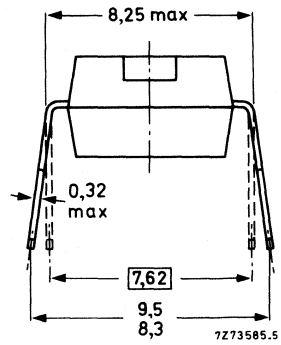
8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)



Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

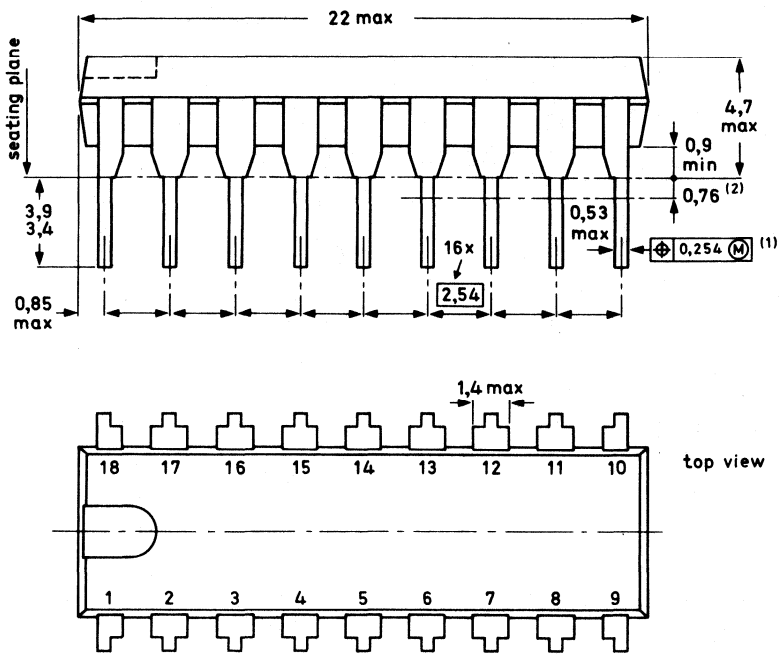
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

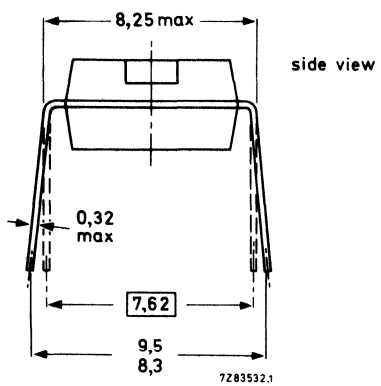
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102H, K, M, PG, RE)





⊕ Positional accuracy.

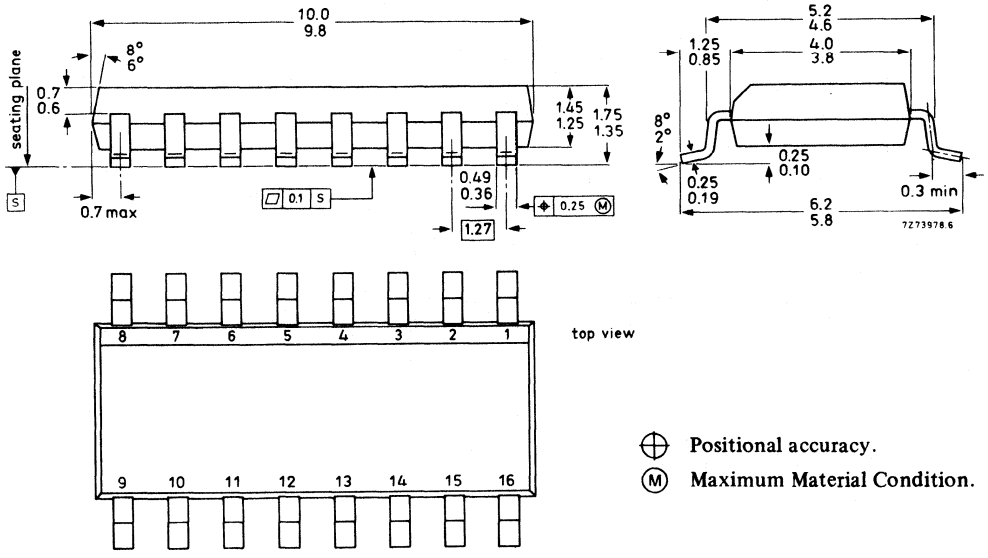
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

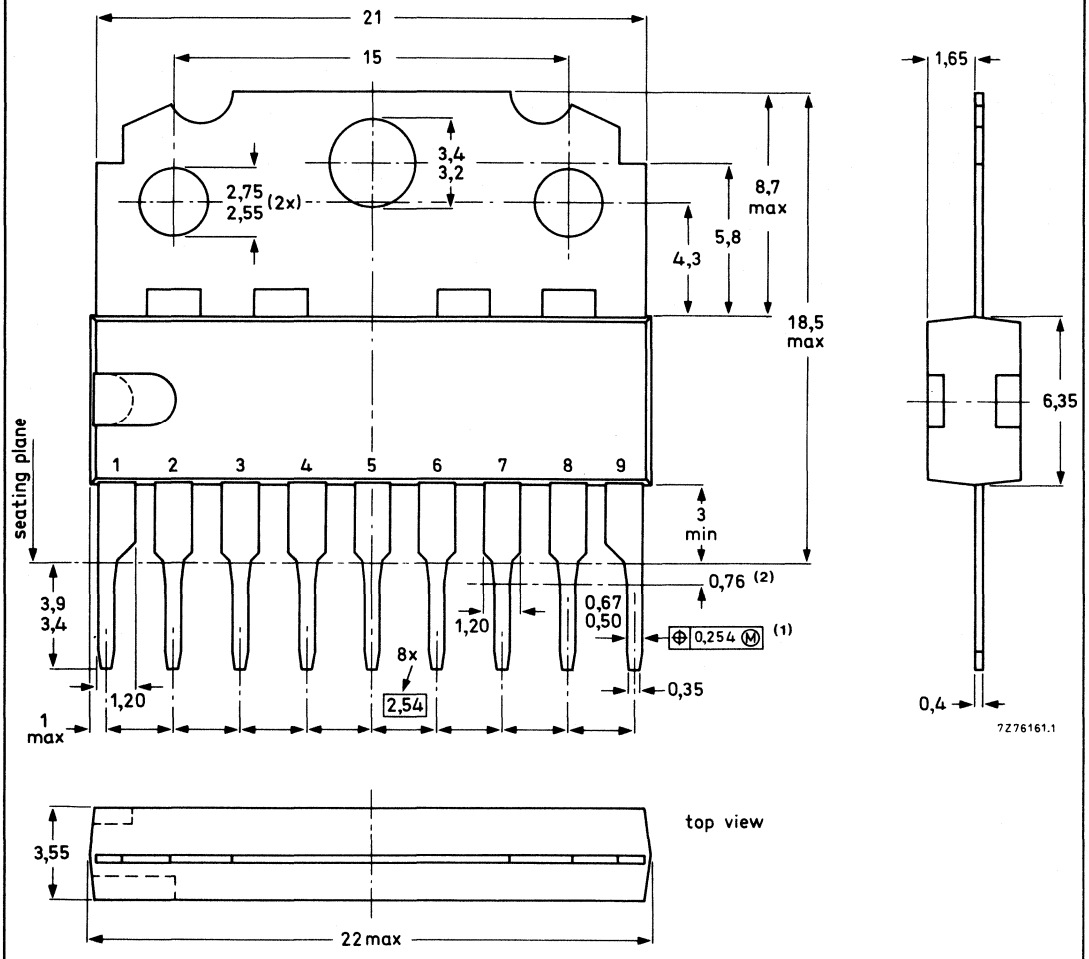


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

NOTES

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to vii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

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